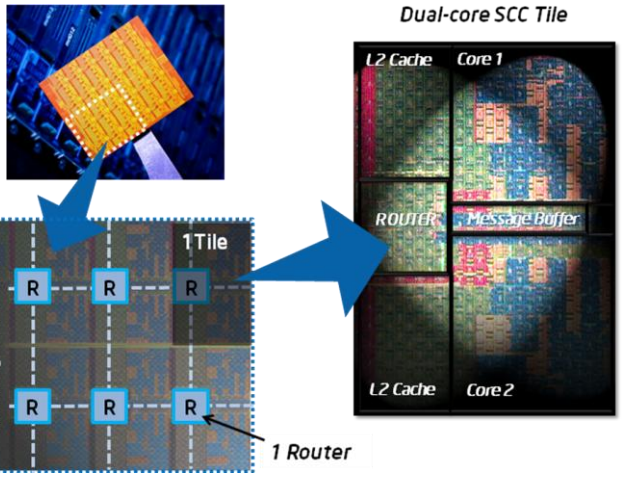
Single-chip Cloud Computer

Intel Labs has created an experimental "Single-chip Cloud Computer," (SCC) a research microprocessor containing the most Intel Architecture cores ever integrated on a silicon CPU chip – 48 cores. It incorporates technologies intended to scale multi-core processors to 100 cores and beyond, such as an on-chip network, advanced power management technologies and support for "message-passing."

Architecturally, the chip resembles a cloud of computers integrated into silicon. The novel many-core architecture includes innovations for scalability in terms of energy-efficiency including improved core-core communication and techniques that enable software to dynamically configure voltage and frequency to attain power consumptions from 125W to as low as 25W.

This represents the latest achievement from Intel's Tera-scale Computing Research Program. The research was co-led by Intel Labs Bangalore, India, Intel Labs Braunschweig, Germany and Intel Labs researchers in the United States.



Anatomy of the Single-chip Cloud Computer

Inside the Single-chip Cloud Computer

The name "Single-chip Cloud Computer" reflects the fact that the architecture resembles a scalable cluster of computers such as you would find in a cloud, integrated into silicon.

The research chip features:

- 24 "tiles" with two IA cores per tile
- A 24-router mesh network with 256 GB/s bisection bandwidth
- 4 integrated DDR3 memory controllers
- Hardware support for message-passing

In a sense, the SCC is a microcosm of cloud datacenter. Each core can run a separate OS and software stack and act like an individual compute node that communicates with other compute nodes over a packet-based network.

One of the most important aspects of the SCC's network fabric architecture is that it supports "scale-out" message-passing programming models that have been proven to scale to 1000s of processors in cloud datacenters. Though each core has 2 levels of cache, there is no hardware cache coherence support among cores in order to simplify the design, reduce power consumption and to encourage the exploration of datacenter distributed memory software models, on-chip. Intel researchers have successfully demonstrated message-passing as well as software-based coherent shared memory on the SCC.

Fine-grained power management is a focus of the chip as well. Software applications are given control to turn cores on and off or to change their performance levels, continuously adapting to use the minimum energy needed at a given moment. The SCC can run all 48 cores at one time over a range of 25W to 125W and selectively vary the voltage and frequency of the mesh network as well as sets of cores. Each tile (2 cores) can have its own frequency, and groupings of four tiles (8 cores) can each run at their own voltage.

A Platform for Software Innovation

Intel Labs believes the SCC is an ideal research platform to help accelerate many-core software research and advanced development. Intel researchers have already ported a variety of applications to the SCC, including web servers, physics modeling, and financial analytics. By the middle of 2010, Intel Labs anticipates having dozens of industry and academic research partners conducting advanced software research on the SCC hardware platform. Visit www.intel.com/go/terascale to find the latest information on this effort.

Learn more at www.intel.com/go/terascale

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