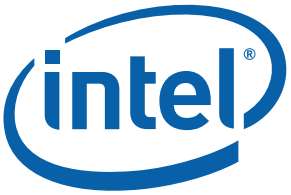

Intel® Xeon® Processor E5-2400 v2 Product Family

Boundary Scan Descriptor Language (BSDL) Readme

January 2014

Reference Number: 329820-001

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Revision History

Document Number	Revision Number	Description	Date
329820	001	• Initial Release	January 2014

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Overview

Scope

This document is intended for the development of IEEE 1149 Boundary scan tests for the Intel® Xeon® Processor E5-2400 v2 Product Family. This readme assumes a working knowledge of IEEE 1149 methodologies and the in circuit test (ICT) manufacturing test methods.

Related Documents

Refer to the following documents for additional processor information.

Table 1. Related Documents

Document	Document Number/Location
Intel® Xeon® Processor E5-2400 v2 Product Family Datasheet - Volume 1	329819-001
Intel® Xeon® Processor E5 v2 Product Family Specification Update	329189-001
IEEE Standard Test Access Port and Boundary Scan Architecture Specification	http://standards.ieee.org

Readme

1. Full Boundary-scan Initialization Requirement

After applying voltage to the power pins, the following initialization sequence must be completed PRIOR to the first TAP accesses during application of the boundary-scan test patterns:

a. BCLK[1:0]_D[P/N] continuous toggle at 100 MHz

b. DRAM_PWR_OK_C[01/23], PWRGOOD, RESET_N are initialized LOW

c. All power supplies are up

d. DRAM_PWR_OK_C[01/23] is driven HIGH and remain driven HIGH during the boundary-scan test pattern execution

e. EAR_N pin is initialized HIGH

f. PROCHOT_N pin is initialized HIGH

g. EAR_N and PROCHOT_N need to be initialized HIGH (de-asserted) before the PWRGOOD assertion.

h. PWRGOOD pin must be driven HIGH 2ms after power pins are stable and remain driven HIGH during the boundary-scan test pattern execution

i. RESET_N pin should be driven LOW for the entire duration of the pattern execution

2. Partial Boundary Scan Initialization Requirement (without DDR cells)

The following alternate initialization sequence does not require BCLK operation, but will disable DDR Boundary-scan functionality. After applying voltage to the power pins, the following initialization sequence must be completed PRIOR to first TAP accesses during application of the boundary-scan test patterns:

a. DRAM_PWR_OK_C[01/23], PWRGOOD, RESET_N are initialized LOW

b. All power supplies are up

c. DRAM_PWR_OK_C[01/23] is driven HIGH and remains driven HIGH during the boundary-scan test pattern execution

d. PWRGOOD pin must be driven HIGH 2ms after power pins are stable and remain driven HIGH during the boundary-scan test pattern execution.

e. RESET_N pin should be driven LOW for the entire duration of pattern execution.

See Figure 1 and Figure 2 for an example test flow.

Figure 1. Test Flow with Partial BSCAN Initialization Example

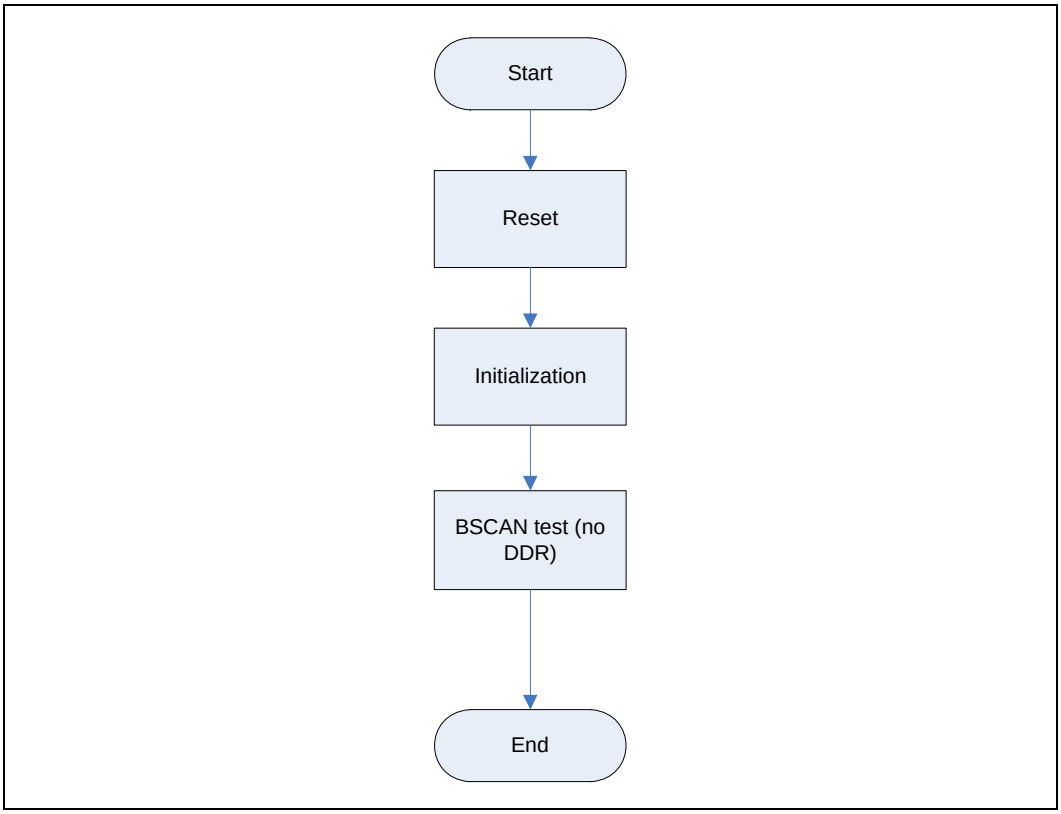
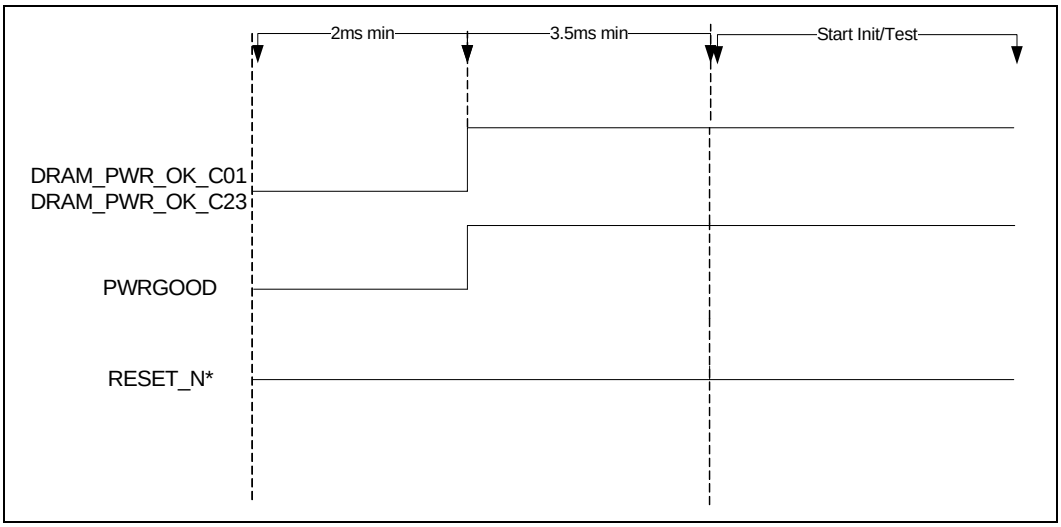


Figure 2. Reset Sequence



Note: *RESET_N should not be held low for the duration of the testing.

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