Networking Interface for Open Programmable Acceleration Engine

Intel FPGA Programmable Acceleration Card D5005

Updated for Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs: 2.0.1
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1. About this Document

1.1. About this Document

This reference manual introduces the IFPGA Rawdev Driver (ifpga_rawdev) that is available for the Intel® FPGA PAC N3000. It introduces the data structures and API functions necessary to use the Intel FPGA PAC N3000 and the Intel Arria® 10 FPGA.

The intended audience for this reference manual is software engineers interested in using and customizing this IFPGA Rawdev Driver. Refer to the existing DPDK documentation for information about other Data Plane Develoment Kit (DPDK) functionality.

1.2. Acronym List

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Expansion</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel FPGA PAC</td>
<td>Intel FPGA Programmable Acceleration Card</td>
<td>Intel FPGA PAC N3000 is a full-duplex 100 Gbps in-system re-programmable acceleration card for multiworkload networking application acceleration.</td>
</tr>
<tr>
<td>AFU</td>
<td>Accelerator Functional Unit</td>
<td>Hardware Accelerator implemented in FPGA logic which offloads a computational operation for an application from the CPU to improve performance.</td>
</tr>
<tr>
<td>AF</td>
<td>Acceleration Function</td>
<td>Compiled Hardware Accelerator image implemented in FPGA logic that accelerates an application.</td>
</tr>
<tr>
<td>API</td>
<td>Application Programming Interface</td>
<td>A set of subroutine definitions, protocols, and tools for building software applications.</td>
</tr>
<tr>
<td>DPDK</td>
<td>Data Plane Development Kit</td>
<td>The Data Plane Development Kit consists of libraries to accelerate packet processing workloads running on many CPU architectures, including x86, POWER and ARM processors. DPDK runs mostly on Linux with a FreeBSD port available for a subset of DPDK features. The Open Source BSD LicenseDPDK licenses DPDK.</td>
</tr>
<tr>
<td>FIU</td>
<td>FPGA Interface Unit</td>
<td>FIU is a platform interface layer that acts as a bridge between platform interfaces like PCIe* and AFU-side interfaces such as CCI-P.</td>
</tr>
<tr>
<td>OPAE</td>
<td>Open Programmable Acceleration Engine</td>
<td>The OPAE is a set of drivers, utilities, and API's for managing and accessing AFs.</td>
</tr>
</tbody>
</table>
2. Overview

The Intel FPGA Programmable Acceleration Card D5005 consists of two QSFP28 networking ports that can be configured for 4x10Gbps operation per port.

Figure 1. Block Diagram: Network Port Feature

The FPGA Interface Manager (FIM) instantiates two Intel Stratix® 10 FPGA Transceiver Native PHY IP cores, one for each QSFP28 network port. The Native PHY IP cores are configured with four transceiver channels, enabling the Accelerator Function (AF) to instantiate an Accelerator Functional Unit (AFU) with up to 8x PRBS Generators and Verifiers, and 8x Reset Controller IP cores.
The Reset Controller IP core orchestrates analog and digital reset signaling for each transceiver channel, as required by the Intel Stratix 10 Native PHY IP core. In a real use case, along with a Reset Controller IP core, you will instantiate the 8x10G PCS and MAC IPs, as well as your user logic in the AF. The raw PHY parallel data interfaces are exposed to the Partial Reconfiguration (PR) boundary through the PR HSSI Interface. The raw PHY interface consists of 80-bit parallel data per transmit or receive direction in each transceiver, along with some sideband signals for handshaking with the Reset Controller IP core across the PR boundary.

The FIM also contains a set of PLLs for each network port. The PLLs provide all the necessary clocks for the transceivers and the AFU. The Memory-Mapped (MM) controllers instantiated in the FIM provide the ability for the software driver to have full access to the Avalon-MM Reconfiguration Interface of the Native PHY IPs through the FPGA Management Engine (FME) registers.

Note: The FIM contains only the Hard PHY in PCS-Direct mode (PMA-only). You implement your own PCS and MAC IP core in the AFU.

Table 1. Correspondence Between Acceleration Stack, FIM, and OPAE Versions

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>2.0.1</td>
<td>9346116d-a52d-5ca8-b06a-a9a389ef7c8d</td>
<td>1.1.4-8</td>
<td>2.0.12</td>
<td>2.0.6</td>
</tr>
<tr>
<td>2.0.1 Beta</td>
<td>8db6b54c-930e-5976-a03b-09f3c913aa95</td>
<td>1.1.4-8</td>
<td>2.0.10</td>
<td>2.0.4</td>
</tr>
<tr>
<td>2.0</td>
<td>bfac4d85-1ee8-56fe-8c95-865ce1bbaa2d</td>
<td>1.1.4-3</td>
<td>1.0.12</td>
<td>1.0.15</td>
</tr>
</tbody>
</table>

Related Information

Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide (PDF)
2.1. Logical View

The FIM instantiates two PLLs that use a 644.53125MHz external reference clock to generate the necessary clocks for the Native PHY IP core and the AFU. The ATX PLL generates the high-speed serial clock for the Native PHY IP core. The fPLL generates two clocks, 322.265625MHz and 161.1328125MHz. Both of the fPLL clocks and RX clocks from the Native PHY IP core are provided to the AFU through the PR HSSI interface.

Figure 2. Logical View of the HSSI PHY
2.2. Physical View

This section depicts the hardware view of a single transceiver channel and its sub-components as part of the Native PHY IP core. The Native PHY IP core is optimized for the lowest roundtrip latency. The Native PHY IP TX/RX PCS-Core Interface FIFOs are configured as following:

- Both QSFP28 Port-0 and Port-1 TX FIFOs are in Phase Compensation mode such that TX clocks can be shared across all 4 channels per QSFP28 interface.
- QSFP28 Port-0 RX FIFO is in Phase Compensation mode.
- QSFP28 Port-1 RX FIFO is in Register mode (bypassed).

Note: In the following figures, the PCS, MAC, and User Logic blocks under AF are shown for illustration. These blocks are not provided by Intel as part of the AFU. Intel only provides an example AFU with 8xPRBS Generators and Verifiers.

Figure 3. Physical View with QSFP28 Port-0
2.3. Clock Architecture

This section describes the clocking architecture of the Native PHY IP core.

All four channels on the TX parallel data interface are clocked by \texttt{f2a\_tx\_parallel\_clk\_x2} clock, per QSFP28 interface. Each one of the four channels on the RX parallel data interface is clocked by its own corresponding \texttt{f2a\_rx\_clkout\[n\]} clock, per QSFP28 interface.

On both the QSFP28 ports, \texttt{tx\_clkout\[n\]} interfaces of the Native PHY IP core have no connection (NC) because the TX FIFO is in Phase Compensation mode and the \texttt{f2a\_tx\_parallel\_clk\_x2} clock is used to drive the \texttt{tx\_coreclkin\[n\]} interfaces.

On the QSFP28 Port-0, \texttt{rx\_coreclkin\[n\]} interfaces of the Native PHY IP core are connected to \texttt{rx\_clkout\[n\]} interfaces because the RX FIFO is in Phase Compensation mode.

On the QSFP28 Port-1, \texttt{rx\_coreclkin\[n\]} interfaces of the Native PHY IP core are connected to ground because the RX FIFO is in Register mode.
Figure 5. Clocking Architecture with QSFP28 Port-0

Figure 6. Clocking Architecture with QSFP28 Port-1

Table 2. Clock Frequencies

<table>
<thead>
<tr>
<th>Clock Name</th>
<th>Frequency in MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>refclk644</td>
<td>644.53125</td>
</tr>
<tr>
<td>rx_cdr_refclk</td>
<td>644.53125</td>
</tr>
<tr>
<td>tx_serial_clk</td>
<td>5156.25</td>
</tr>
<tr>
<td>f2a_tx_parallel_clk_x1</td>
<td>161.1328125</td>
</tr>
</tbody>
</table>

**continued...**
<table>
<thead>
<tr>
<th>Clock Name</th>
<th>Frequency in MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>f2a_tx_parallel_clk_x2</td>
<td>322.265625</td>
</tr>
<tr>
<td>tx_clkout[n]</td>
<td>322.265625</td>
</tr>
<tr>
<td>tx_coreclkin[n]</td>
<td>322.265625</td>
</tr>
<tr>
<td>rx_clkout[n]</td>
<td>322.265625</td>
</tr>
<tr>
<td>rx_coreclkin[n]</td>
<td>322.265625</td>
</tr>
</tbody>
</table>

You can access the following clocks from AF:

- rx_clkout[n]
- f2a_tx_parallel_clk_x1
- f2a_tx_parallel_clk_x2

**Clock Relationship**

- The refclk644, external reference clocks, come from different sources for each QSFP28 network port. Therefore, the relationship between any given clock on network port 0 is asynchronous to any given clock on network port 1.
- The f2a_tx_parallel_clk_x1 and f2a_tx_parallel_clk_x2 are phase synchronous for a given QSFP28 network port.
- The rx_clkout[n] clocks are recovered by the Clock and Data Recovery (CDR) unit in the receiver of each channel. All the rx_clkout[n] clocks are asynchronous to one another.
3. Partial Reconfiguration HSSI Interface

The Partial Reconfiguration (PR) HSSI interface is a unified data interface that connects a network port to the PRBS Generators and Verifiers. The unified data interface consists of a fixed set of physical ports that are mapped to specific signaling functions. The PR HSSI interface also provides clocks for synchronization as well as control and status signals for analog and digital reset sequence orchestration between the PHY in FIM and the reset controller IP core in AF. The figure below provides a high-level block diagram for one QSFP instance.

![PR HSSI Block Diagram](image)

3.1. Clock Signals

The clocks of the PR HSSI Interface synchronize the unified data interface between the PRBS Generators and Verifiers, and the HSSI PHY. The signal directions listed for HSSI ports are from the perspective of the FIM. The signals listed below are identical for both QSFP28 interfaces.
Table 3.  Clock Signals

<table>
<thead>
<tr>
<th>Port Name</th>
<th>Width</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>f2a_tx_parallel_clk_x1</td>
<td>1</td>
<td>Output</td>
<td>A 161.1328125 MHz clock generated by an fPLL in the HSSI PHY from a 644.53125 MHz QSFP28 external reference clock. This clock is intended to drive the user logic in the AF.</td>
</tr>
<tr>
<td>f2a_tx_parallel_clk_x2</td>
<td>1</td>
<td>Output</td>
<td>A 322.265625 MHz clock generated by an fPLL in the HSSI PHY from a 644.53125 MHz QSFP28 external reference clock. This clock drives the tx_coreclkin inputs of all 4 channels of the Native PHY IP core. All transmit data from AFU to HSSI PHY should be synchronous to f2a_tx_parallel_clk_x2.</td>
</tr>
<tr>
<td>f2a_rx_clkout</td>
<td>4</td>
<td>Output</td>
<td>A 322.265625 MHz clock at the output of the Native PHY IP core tx_clkout[n] interface. All receive data to the PRBS Verifiers from the HSSI PHY is synchronous to f2a_rx_clkout[n], per transceiver channel n.</td>
</tr>
</tbody>
</table>

3.2. Data Interface and Signals

The HSSI unified data interface conforms to the Intel Stratix 10 FPGA Transceiver Native PHY IP core configured in 32-bit PCS-Direct mode. It consists of generic parallel data and encoding control interfaces for transmit and receive that are mapped to specific signaling behavior as outlined in the *Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide*. The unified data interface also includes flow control ports to manage passing data to and from the HSSI PHY interface.

The table below provides a cross reference from the hssi:raw_pr unified data interface signals to the Intel Stratix 10 FPGA Transceiver Native PHY IP core with enhanced PCS signal set. The HSSI PHY IP is configured in Configuration-32, PMA width-32, FPGA Fabric width-32. The TX Core FIFO is configured in Phase Compensation mode. The RX Core FIFO QSFP0 is configured in Phase Compensation mode and RX Core FIFO QSFP1 is configured in Register mode. The Simplified Data Interface is disabled. The Double-Rate Transfer is disabled. For detailed information on these signals, refer to the *Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide*.

Table 4.  Data Signals

<table>
<thead>
<tr>
<th>Port Name</th>
<th>Width</th>
<th>Direction</th>
<th>Clock Domain</th>
<th>Native PHY IP Port Name</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PCS-Core Interface Ports: PCS-Direct</td>
</tr>
<tr>
<td>a2f_tx_parallel_data</td>
<td>4*80</td>
<td>Input</td>
<td>f2a_tx_parallel_clk_x2</td>
<td>tx_parallel_data</td>
<td></td>
</tr>
<tr>
<td>f2a_rx_parallel_data</td>
<td>4*80</td>
<td>Output</td>
<td>f2a_rx_clkout[n]</td>
<td>rx_parallel_data</td>
<td></td>
</tr>
<tr>
<td>f2a_tx_fifo_empty</td>
<td>4</td>
<td>Output</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>f2a_tx_fifo_full</td>
<td>4</td>
<td>Output</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>f2a_tx_fifo_pempty</td>
<td>4</td>
<td>Output</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>f2a_tx_fifo_pfull</td>
<td>4</td>
<td>Output</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Continued...
3.3. Control and Status Signals

The PR HSSI Interface provides signals for HSSI PHY PCS status and transceiver loopback control. The signal behavior conforms to the Intel Stratix 10 FPGA Transceiver Native PHY IP core in 32-bit PCS-Direct mode. The below table cross references the HSSI port names to the Native PHY IP port names.

Table 5. Control and Status Signals

<table>
<thead>
<tr>
<th>hssi Port Name</th>
<th>Width</th>
<th>Direction</th>
<th>Clock Domain</th>
<th>Native PHY IP Core Port Name</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>f2a_tx_ready</td>
<td>4</td>
<td>Output</td>
<td>Asynchronous</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>f2a_rx_ready</td>
<td>4</td>
<td>Output</td>
<td>Asynchronous</td>
<td>tx_cal_busy</td>
<td>-</td>
</tr>
<tr>
<td>a2f_rx_seriallpbken</td>
<td>4</td>
<td>Input</td>
<td>Asynchronous</td>
<td>rx_seriallpbken</td>
<td>-</td>
</tr>
<tr>
<td>f2a_atxpll_locked</td>
<td>1</td>
<td>Output</td>
<td>Asynchronous</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>f2a_fpll_locked</td>
<td>1</td>
<td>Output</td>
<td>Asynchronous</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>f2a_tx_cal_busy</td>
<td>4</td>
<td>Output</td>
<td>Asynchronous</td>
<td>tx_cal_busy</td>
<td>-</td>
</tr>
<tr>
<td>f2a_rx_cal_busy</td>
<td>4</td>
<td>Output</td>
<td>Asynchronous</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>f2a_rx_is_lockedtodata</td>
<td>4</td>
<td>Output</td>
<td>Synchronous to CDR</td>
<td>rx_is_lockedtodata</td>
<td>-</td>
</tr>
<tr>
<td>f2a_rx_is_lockedorf</td>
<td>4</td>
<td>Output</td>
<td>f2a_rx_clkout[n]</td>
<td>rx_is_lockedorf</td>
<td>-</td>
</tr>
<tr>
<td>a2f_tx_analogreset</td>
<td>4</td>
<td>Input</td>
<td>Synchronous to Reset Controller IP input clock (recommended 100-125MHz)</td>
<td>tx_analogreset</td>
<td>-</td>
</tr>
</tbody>
</table>

Related Information
Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide (PDF)
### 3.4. Connecting the PCS to the HSSI Interface

In 32-bit PCS-Direct mode, the interface between the PCS and HSSI PHY maps as following:

**Table 6. Interface Mapping**

<table>
<thead>
<tr>
<th>TX Port Function</th>
<th>TX Port</th>
<th>RX Port Function</th>
<th>RX Port</th>
</tr>
</thead>
<tbody>
<tr>
<td>data[31:0]</td>
<td>tx_parallel_data[31:0]</td>
<td>data[31:0]</td>
<td>rx_parallel_data[31:0]</td>
</tr>
<tr>
<td>tx_fifo_wr_en</td>
<td>tx_parallel_data[79]</td>
<td>rx_prbs_err</td>
<td>rx_parallel_data[35]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>rx_prbs_done</td>
<td>rx_parallel_data[36]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>rx_data_valid</td>
<td>rx_parallel_data[79]</td>
</tr>
</tbody>
</table>
Figure 8. Connecting the PCS to the HSSI Interface

This figure illustrates how to connect a 10GbE PCS to the HSSI PHY using the PR HSSI Interface.

<table>
<thead>
<tr>
<th>n(^{th}) 10GbE PCS Instance on QSFP28 Port 0 or 1 (n = 0, 1, 2, 3)</th>
<th>PR HSSI Interface</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clocks</td>
<td>Clocks</td>
</tr>
<tr>
<td>XGMII or Parallel Data Interface</td>
<td>Unified Data Interface</td>
</tr>
<tr>
<td>PHY Control and Status</td>
<td>PHY Control and Status</td>
</tr>
</tbody>
</table>

- a2f\(_{tx}\)\(_{parallel}\)_\(data[(n*80) + 79 : (n*80)]\)
- f2a\(_{tx}\)_\(fifo\)_\(empty\)[n]
- f2a\(_{tx}\)_\(fifo\)_\(full\)[n]
- f2a\(_{tx}\)_\(fifo\)_\(pempty\)[n]
- f2a\(_{tx}\)_\(fifo\)_\(pfull\)[n]
- f2a\(_{tx}\)_\(tx\)_\(fifo\)_\(pempty\)[n]
- f2a\(_{tx}\)_\(tx\)_\(fifo\)_\(pfull\)[n]
- f2a\(_{tx}\)_\(tx\)_\(ready\)[n]
- f2a\(_{tx}\)_\(tx\)_\(ready\)[n]
- f2a\(_{tx}\)_\(tx\)_\(tx\)_\(analogreset\)[n]
- f2a\(_{tx}\)_\(tx\)_\(tx\)_\(analogreset\)[n]
- f2a\(_{tx}\)_\(tx\)_\(tx\)_\(analogreset\)[n]
- f2a\(_{tx}\)_\(tx\)_\(tx\)_\(analogreset\)[n]
- f2a\(_{tx}\)_\(tx\)_\(tx\)_\(analogreset\)[n]
- f2a\(_{tx}\)_\(tx\)_\(tx\)_\(analogreset\)[n]

- f2a\(_{rx}\)_\(fifo\)_\(empty\)[n]
- f2a\(_{rx}\)_\(fifo\)_\(full\)[n]
- f2a\(_{rx}\)_\(fifo\)_\(pempty\)[n]
- f2a\(_{rx}\)_\(fifo\)_\(pfull\)[n]
- f2a\(_{rx}\)_\(rx\)_\(fifo\)_\(pfull\)[n]
- f2a\(_{rx}\)_\(rx\)_\(fifo\)_\(pempty\)[n]
- f2a\(_{rx}\)_\(rx\)_\(fifo\)_\(rd\)_\(en\)[n]

- a2f\(_{tx}\)_\(tx\)_\(analogreset\)[n]
- a2f\(_{tx}\)_\(tx\)_\(digitalreset\)[n]
- a2f\(_{tx}\)_\(tx\)_\(digitalreset\)[n]
- a2f\(_{tx}\)_\(tx\)_\(digitalreset\)[n]

NC = No connection
4. Native PHY IP Core Parameters

During the FIM instantiation, the following IP parameters were selected for generating the PHY IP core. These parameter settings are informative, you can not control or configure them. For more information about these parameters, refer to the Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide.

Figure 9. Category: General

![General Configuration](image)

Figure 10. Category: TX PMA

![TX PMA Configuration](image)
4. Native PHY IP Core Parameters

**Figure 11.** Category: RX PMA

![RX CDR Options](image_url)

- Number of CDR reference clocks: 1
- Selected CDR reference clock: 0
- Selected CDR reference clock frequency: 644.531250 MHz
- PPM detector threshold: 1000 PPM

**Figure 12.** Category: PCS-Direct

![PCS Direct interface width](image_url)

- PCS Direct interface width: 32
Figure 13. Category: PCS Core Interface

**General Interface Options**
- Enable PCS reset status ports

**TX PCS-Core Interface FIFO**
- TX Core Interface FIFO mode: Phase compensation
- TX FIFO partially full threshold: 5
- TX FIFO partially empty threshold: 2
  - Enable tx_fifo_full port
  - Enable tx_fifo_empty port
  - Enable tx_fifo_pfull port
  - Enable tx_fifo_pempty port
  - Enable tx_dlllock port

**RX PCS-Core Interface FIFO**
- RX PCS-Core Interface FIFO mode (PCS FIFO-Core FIFO): Register
- RX FIFO partially full threshold: 5
- RX FIFO partially empty threshold: 2
  - Enable RX FIFO alignment word deletion (Interlaken)
  - Enable RX FIFO control word deletion (Interlaken)
  - Enable rx_data_valid port
  - Enable rx_fifo_full port
  - Enable rx_fifo_empty port
  - Enable rx_fifo_pfull port
  - Enable rx_fifo_pempty port
  - Enable rx_fifo_del port (10GBASE-R)
  - Enable rx_fifo_insert port (10GBASE-R)
  - Enable rx_fifo_rd_en port
  - Enable rx_fifo_align_clr port (Interlaken)

**TX Clock Options**
- Selected tx_clkout clock source: PCS clkout
- Enable tx_clkout2 port
- Selected tx_clkout2 clock source: PCS clkout
- TX pma_div_clkout division factor:
- Selected tx_coreclk1n clock network: Dedicated Clock
  - Enable tx_coreclk1n port

**RX Clock Options**
- Selected rx_clkout clock source: PCS clkout x2
- Enable rx_clkout2 port
- Selected rx_clkout2 clock source: PCS clkout
- RX pma_div_clkout division factor: 2
- Selected rx_coreclk1n clock network: Dedicated Clock

**Latency Measurement Options**
- Enable latency measurement ports
Figure 14. Category: Analog PMA Setting
**Figure 15. Category: ATX PLL IP Setting**

- **General**
  - Message level for rule violations:
  - Protocol mode:
  - Bandwidth:
  - Number of PLL reference clocks:
  - Selected reference clock source:
  - VCCAUX and VCCINT supply voltage for the Transceiver:

- **Note**: All PLLs and Native PHY instances in a given tile must be configured with the same supply voltage.

- **Ports**
  - Primary PLL clock output buffer:
  - RX clock output buffer:
  - Enable RX clock output port (ts_serial_clk)
  - Enable RX clock output port to above ATX PLL (pctrl_output_to_ser_ser)
  - Enable RX clock output port to below ATX PLL (pctrl_output_to_ser_ser)
  - Enable RX local clock output port (ts_serial_clk_out)
  - Enable RX clock input port from above ATX PLL (pctrl_input_from_ser_ser)
  - Enable RX clock input port from below ATX PLL (pctrl_input_from_ser_ser)
  - Enable PCIe clock output port
  - Enable ATX to FPLL cascade clock output port

- **GTX Configuration Options**
  - Enable GTX clock buffer to above ATX PLL
  - Enable GTX clock buffer to below ATX PLL
  - GTX output clock source:

- **Output Frequency**
  - PLL output frequency: 51.5625 MHz
  - PLL output datarate: 1.03125 Mbps
  - PLL auto mode reference clock frequency (integer): 64.53125 MHz
  - Configure counters manually
  - Multiply factor (N-Counter):
  - Divide factor (N-Counter):
  - Divide factor (L-Counter):

- **MCGB**
  - Include Master Clock Generation Block
  - Clock division factor:
  - Enable x24 non-bonded high-speed clock output port
  - Enable PCIe clock switch interface
  - Enable mcgbrst and mcgbrstat ports
  - Number of auxiliary MCGB clock input ports:
  - MCGB input clock frequency: 1,031.25 MHz
  - MCGB output data rate: 1.03125 Mbps

- **Bonding**
  - Enable bonding clock output ports
  - PMA interface width:

<table>
<thead>
<tr>
<th>Parameter Names</th>
<th>Parameter Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMA rate</td>
<td>1.03125 Mbps</td>
</tr>
<tr>
<td>L counter (valid in frac)</td>
<td>1</td>
</tr>
<tr>
<td>L cascade counter (valid)</td>
<td>0</td>
</tr>
<tr>
<td>L cascade pred.</td>
<td>select_ycc_output</td>
</tr>
<tr>
<td>N counter</td>
<td>1</td>
</tr>
<tr>
<td>PLL output frequency</td>
<td>51.5625 MHz</td>
</tr>
<tr>
<td>vcc_freq</td>
<td>1.03125 MHz</td>
</tr>
</tbody>
</table>
Figure 16.  Category: fPLL IP Setting

Related Information
Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide (PDF)
5. OPAE Support

The OPAE SDK includes the following support for the Intel FPGA PAC D5005 network port feature:

- OPAE kernel driver sysfs files enable configuration of the network port feature and allows access to related information on the Intel FPGA PAC D5005 from the host.
  - 128-bit UUID
  - HSSI PHY PMA analog settings

5.1. Supported Settings

The OPAE driver is capable of changing the following transmitter settings per transceiver channel:

- Pre-emphasis
- TX Output Differential Swing (VOD)
- TX Compensation

For more information, refer to the Transmitter PMA Logical Register Map.

5.2. Unsupported Settings

The OPAE driver is not capable of changing the following settings:

- Transmitter Slew Rate
- PMA Receiver Settings (VGA, CTLE, DFE, Adaptation Modes)

5.3. Tuning Information

Before you proceed further, you must install and load the OPAE driver and tools. For more information, refer to the Intel Acceleration Stack Quick Start Guide: Intel FPGA Programmable Acceleration Card D5005.

sysfs Tree

Sysfs entries allow reading or writing to HSSI configuration and status registers (CSR):

/sys/class/fpga/intel-fpga-dev.0/intel-fpga-fme.0/intel-pac-hssi.<1/2>.auto/

The HSSI sysfs tree is as follows:
• qsfp<0/1>
  — ctrl HSSI_CTRL_QSFP<0/1> CSR: allows access to control registers
  — stat HSSI_STAT_QSFP<0/1> CSR: allows access to status registers
  — chan<0/1/2/3>: analog settings of each of the 4 transceiver channels per QSFP interface
    • tx_post_tap: Pre-emphasis 1st post-tap magnitude and polarity
    • tx_pre_tap: Pre-emphasis 1st pre-tap magnitude and polarity
    • tx_vod: TX output differential swing
    • tx_comp: TX Compensation

**tx_post_tap**

• Use tx_post_tap sysfs entry to tune the transmitter pre-emphasis 1st post-tap magnitude and polarity.
• Valid magnitude is between -24 and 24.
To evaluate the correct setting, refer to the Intel Stratix 10 H-tile Pre-Emphasis and Output Swing Estimator.

**Example:**

1. Change directory to the desired QSFP interface and channel:

   ```
   $ cd /sys/class/fpga/intel-fpga-dev.0/intel-fpga-fme.0/intel-pac-hssi.<1/2>.auto/qsfp<0/1>/chan<0/1/2/3>
   ```

2. Read current tx_post_tap setting:

   ```
   $ cat tx_post_tap
   Output: 0
   ```

3. Write new tx_post_tap magnitude and polarity, assume it as magnitude of 1 with positive polarity:

   ```
   $ sudo -- sh -c 'echo +1 > tx_post_tap'
   ```

4. Verify that tx_post_tap:

   ```
   $ cat tx_post_tap
   Output: +1
   ```

**tx_pre_tap**

• Use tx_pre_tap sysfs entry to tune the transmitter pre-emphasis 1st pre-tap magnitude and polarity.
• Valid magnitude is between -15 and 15.
To evaluate the correct setting, refer to the Intel Stratix 10 H-tile Pre-Emphasis and Output Swing Estimator. Also, refer to the example under tx_post_tap.
**tx_vod**

- Use `tx_vod` sysfs entry to tune the transmitter output differential swing.
- Valid output swing level is between 17 (600 mV) and 31 (VCCT or Transmitter Power Supply Voltage)

To evaluate the correct setting, refer to the Intel Stratix 10 H-tile Pre-Emphasis and Output Swing Estimator.

**Example:**

1. Change directory to the desired QSFP interface and channel:
   ```
   $ cd /sys/class/fpga/intel-fpga-dev.0/intel-fpga-fme.0/intel-pac-hssi.<1/2>.auto/qsfp<0/1>/chan<0/1/2/3>
   ```

2. Read current `tx_vod` setting:
   ```
   $ cat tx_vod
   Output: 31
   ```

3. Write new `tx_vod` output, assume it as 29:
   ```
   $ sudo -- sh -c 'echo 29 > tx_vod'
   ```

4. Verify that `tx_vod`:
   ```
   $ cat tx_vod
   Output: 29
   ```

**tx_comp**

- Use `tx_comp` sysfs entry to tune the transmitter compensation, which helps reduce the PDN induced ISI jitter when enabled.
- Valid compensation value is either 0 (off) or 1 (on)

**Example:**

1. Change directory to the desired QSFP interface and channel:
   ```
   $ cd /sys/class/fpga/intel-fpga-dev.0/intel-fpga-fme.0/intel-pac-hssi.<1/2>.auto/qsfp<0/1>/chan<0/1/2/3>
   ```

2. Read current `tx_comp` setting:
   ```
   $ cat tx_comp
   Output: 1
   ```

3. TX compensation is currently enabled, let's turn it off:
   ```
   $ sudo -- sh -c 'echo 0 > tx_comp'
   ```

4. Verify that `tx_comp`:
   ```
   $ cat tx_comp
   Output: 0
   ```
Monitor `dmesg` for Errors

Example: Error in setting the transmitter output differential swing to 100

```bash
$ echo 100 > tx_vod
bash: echo: write error: Invalid argument
```

Check `dmesg`

```bash
$ dmesg
[ 7597.306591] intel-pac-hssi intel-pac-hssi.2.auto: Max VOD is 31
```

Example: Error in setting a legal tx_vod value

```bash
$ echo 31 > tx_vod
bash: echo: write error: Connection timed out
```

Check `dmesg`

```bash
$ dmesg
[ 7812.184357] intel-pac-hssi intel-pac-hssi.2.auto: timeout, HSSI ack not received
```

Check if the channel is held in reset

```bash
$ cat stat
0x000f000f000f000f
```

Deassert the reset

```bash
$ echo 0x0 > ctrl
$ cat stat
0xf3c0f3c0f3c0f3c0
```
## 6. Document Revision History for Networking Interface for OPAE

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Acceleration Stack Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| 2019.11.04       | 2.0.1 (compatible with Intel Quartus® Prime Pro Edition 19.2) | Updated the entire document to reflect:  
  - Addition of the PHY PCS-direct mode and hssi_PRBS AFU support.  
  - Removal of the 10GbE MAC AFU support. |
| 2019.08.05       | 2.0 (compatible with Intel Quartus Prime Pro Edition 18.1.2) | Initial release. |