Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2	Board Connection Requirement for Pin Migration Only
3A		TDO		TDO			AD25				
3A		nCSO		DATA4			AD24				
3A		TMS		TMS			AE25				
3A		AS_DATA3		DATA3			AE24				
3A		TCK		TCK			AC22				
3A		AS_DATA2		DATA2			AB21				
3A		TDI		TDI			AD23				
3A		AS_DATA1		DATA1			AE21				
3A		DCLK		DCLK			AE22				
3A		AS_DATA0,ASDO		DATA0			AE23				
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	AE18	DQ1B			
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	AE20				
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	AD19	DQ1B			
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	AD21	DQ1B			
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	AD18	DQSn1B			
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	AB20	DQ1B			
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	AC17	DQS1B			
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	AB19				
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	AE17	DQ1B			
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	AC19	DQ1B			
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	AD16	DQ1B			
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	AC18	DQ1B			
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	AE16				
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	AB17	DQ1B			
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	AE15				
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AA17	DQ1B			
3B	VREFB3BN0	IO			DIFFIO_RX_B10n	DIFFOUT_B10n	AA16				
3B	VREFB3BN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	AC16				
3B	VREFB3BN0	IO			DIFFIO_RX_B14n	DIFFOUT_B14n	AB15				
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B15n	DIFFOUT_B15n	AD15				
3B	VREFB3BN0	IO	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B15p	DIFFOUT_B15p	AD14				
3B	VREFB3BN0	IO			DIFFIO_TX_B17n	DIFFOUT_B17n	AB14				
3B	VREFB3BN0	IO			DIFFIO_RX_B18n	DIFFOUT_B18n	AE13	DQ2B			
3B	VREFB3BN0	IO			DIFFIO_TX_B17p	DIFFOUT_B17p	AA14	DQ2B			
3B	VREFB3BN0	IO			DIFFIO_RX_B18p	DIFFOUT_B18p	AE12	DQ2B			
3B	VREFB3BN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	AE11	DQSn2B			
3B	VREFB3BN0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	AD13	DQ2B			
3B	VREFB3BN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	AE10	DQS2B			
3B	VREFB3BN0	IO			DIFFIO_TX_B20p	DIFFOUT_B20p	AC14				
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B21n	DIFFOUT_B21n	AB12	DQ2B			
3B	VREFB3BN0	IO			DIFFIO_RX_B22n	DIFFOUT_B22n	AD11	DQ2B			
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p	DIFFOUT_B21p	AA12	DQ2B			
3B	VREFB3BN0	IO			DIFFIO_RX_B22p	DIFFOUT_B22p	AC12	DQ2B			
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B23n	DIFFOUT_B23n	AD10				
3B	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	AB11	DQ2B			
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B23p	DIFFOUT_B23p	AD9				
3B	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	AA11	DQ2B			
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B25n	DIFFOUT_B25n	AB10				
4A	VREFB4AN0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	AE8	DQ3B			
4A	VREFB4AN0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	AA9	DQ3B			
4A	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	AD8	DQ3B			
4A	VREFB4AN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	AC9	DQSn3B			
4A	VREFB4AN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AB9	DQ3B			
4A	VREFB4AN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	AC8	DQS3B			
4A	VREFB4AN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AA8				
4A	VREFB4AN0	IO			DIFFIO_TX_B29n	DIFFOUT_B29n	AC7	DQ3B			
4A	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	AE6	DQ3B			
4A	VREFB4AN0	IO			DIFFIO_TX_B29p	DIFFOUT_B29p	AC6	DQ3B			
4A	VREFB4AN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	AD6	DQ3B			
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B31n	DIFFOUT_B31n	AE5				
4A	VREFB4AN0	IO			DIFFIO_TX_B32n	DIFFOUT_B32n	AC4	DQ3B			
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B31p	DIFFOUT_B31p	AD5				
4A	VREFB4AN0	IO			DIFFIO_TX_B32p	DIFFOUT_B32p	AB5	DQ3B			
4A	VREFB4AN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AC3				
4A	VREFB4AN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AE3	DQ4B			
4A	VREFB4AN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AB4	DQ4B			
4A	VREFB4AN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AE2	DQ4B			
4A	VREFB4AN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	AD4	DQSn4B			
4A	VREFB4AN0	IO			DIFFIO_TX_B36n	DIFFOUT_B36n	AA4	DQ4B			
4A	VREFB4AN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	AD3	DQS4B			
4A	VREFB4AN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	AA3				
4A	VREFB4AN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	W3	DQ4B			
4A	VREFB4AN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AE1	DQ4B			
4A	VREFB4AN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	V4	DQ4B			
4A	VREFB4AN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AD1	DQ4B			
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B39n	DIFFOUT_B39n	AC2				
4A	VREFB4AN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	Y3	DQ4B			
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B39p	DIFFOUT_B39p	AC1				
4A	VREFB4AN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	W4	DQ4B			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2	Board Connection Requirement for Pin Migration Only
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	AB2				
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	AB1				
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AA2				
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	Y2				
4A	VREFB4AN0	IO			DIFFIO_RX_B47n	DIFFOUT_B47n	Y1				
4A	VREFB4AN0	IO			DIFFIO_RX_B47p	DIFFOUT_B47p	W1				
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	U2	DQ1R			
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	V2				
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	U1	DQ1R			
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	V1				
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	T4	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	R2	DQ1R			
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	R3	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	T2	DQ1R			
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	P3				
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	P1	DQS1R			
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	N2	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	R1	DQSn1R			
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	N4	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	M1	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	N3				
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	N1	DQ1R			
5B	VREFB5BN0	IO	CLK6p		DIFFIO_RX_R17p	DIFFOUT_R17p	L2				
5B	VREFB5BN0	IO	CLK6n		DIFFIO_RX_R17n	DIFFOUT_R17n	M2				
5B	VREFB5BN0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	K2				
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R20p	DIFFOUT_R20p	M4				
5B	VREFB5BN0	IO			DIFFIO_RX_R19n	DIFFOUT_R19n	K1				
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R20n	DIFFOUT_R20n	L3				
5B	VREFB5BN0	IO			DIFFIO_RX_R21p	DIFFOUT_R21p	H1				
5B	VREFB5BN0	IO			DIFFIO_TX_R22p	DIFFOUT_R22p	J4				
5B	VREFB5BN0	IO			DIFFIO_RX_R21n	DIFFOUT_R21n	J1				
5B	VREFB5BN0	IO			DIFFIO_TX_R22n	DIFFOUT_R22n	J3				
5B	VREFB5BN0	IO			DIFFIO_RX_R23p	DIFFOUT_R23p	H2				
5B	VREFB5BN0	IO			DIFFIO_TX_R24p	DIFFOUT_R24p	H4				
5B	VREFB5BN0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	G1				
5B	VREFB5BN0	IO			DIFFIO_TX_R24n	DIFFOUT_R24n	H3				
		GND					F3				
7A	VREFB7AN0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	E1		GND	GND	
7A	VREFB7AN0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	D1		GND	GND	
7A	VREFB7AN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	F2				
7A	VREFB7AN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	E2				
7A	VREFB7AN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	F4		T_RESET#	T_RESET#	
7A	VREFB7AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	E3				
7A	VREFB7AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	D3				
7A	VREFB7AN0	IO	CLK11p		DIFFIO_RX_T25p	DIFFOUT_T25p	C1				
7A	VREFB7AN0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	C7	DQ1T	T_DM_1	T_DM_1	
7A	VREFB7AN0	IO	CLK11n		DIFFIO_RX_T25n	DIFFOUT_T25n	B1				
7A	VREFB7AN0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	C6	DQ1T	T_DQ_15	T_DQ_15	
7A	VREFB7AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	C3	DQ1T	T_DQ_13	T_DQ_13	
7A	VREFB7AN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	D4	DQ1T	T_DQ_14	T_DQ_14	
7A	VREFB7AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	C2	DQ1T	T_DQ_12	T_DQ_12	
7A	VREFB7AN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	C4	DQ1T	T_CKE_0	T_CKE_0	
7A	VREFB7AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	B2	DQS1T	T_DQS_1	T_DQS_1	
7A	VREFB7AN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	D8		T_CKE_1	T_CKE_1	
7A	VREFB7AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	A2	DQSn1T	T_DQS#_1	T_DQS#_1	
7A	VREFB7AN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	C8	DQ1T	T_DQ_11	T_DQ_11	
7A	VREFB7AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	A4	DQ1T	T_DQ_9	T_DQ_9	
7A	VREFB7AN0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	B5	DQ1T	T_DQ_10	T_DQ_10	
7A	VREFB7AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	A3	DQ1T	T_DQ_8	T_DQ_8	
7A	VREFB7AN0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	B4		GND	GND	
7A	VREFB7AN0	IO	CLK10p		DIFFIO_RX_T33p	DIFFOUT_T33p	B6				
7A	VREFB7AN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	E8	DQ2T	T_DM_0	T_DM_0	
7A	VREFB7AN0	IO	CLK10n		DIFFIO_RX_T33n	DIFFOUT_T33n	A5				
7A	VREFB7AN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	D9	DQ2T	T_DQ_7	T_DQ_7	
7A	VREFB7AN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	B7	DQ2T	T_DQ_5	T_DQ_5	
7A	VREFB7AN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	E10	DQ2T	T_DQ_6	T_DQ_6	
7A	VREFB7AN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	A7	DQ2T	T_DQ_4	T_DQ_4	
7A	VREFB7AN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	D10	DQ2T	T_ODT_1	T_ODT_1	
7A	VREFB7AN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	A9	DQS2T	T_DQS_0	T_DQS_0	
7A	VREFB7AN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	E11		T_ODT_0	T_ODT_0	
7A	VREFB7AN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	A8	DQSn2T	T_DQS#_0	T_DQS#_0	
7A	VREFB7AN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	D11	DQ2T	T_DQ_3	T_DQ_3	
7A	VREFB7AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	B9	DQ2T	T_DQ_1	T_DQ_1	
7A	VREFB7AN0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	C11	DQ2T	T_DQ_2	T_DQ_2	
7A	VREFB7AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	A10	DQ2T	T_DQ_0	T_DQ_0	
7A	VREFB7AN0	IO	RZQ_2		DIFFIO_TX_T40n	DIFFOUT_T40n	B10				
8A	VREFB8AN0	IO	CLK9p		DIFFIO_RX_T41p	DIFFOUT_T41p	B12				
8A	VREFB8AN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	E13	DQ3T	T_A_0	T_CA_0	
8A	VREFB8AN0	IO	CLK9n		DIFFIO_RX_T41n	DIFFOUT_T41n	A12				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2	Board Connection Requirement for Pin Migration Only
8A	VREFB8AN0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	D14	DQ3T	T_A_1	T_CA_1	
8A	VREFB8AN0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	A14	DQ3T	T_A_4	T_CA_4	
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T44p	DIFFOUT_T44p	E15	DQ3T	T_A_2	T_CA_2	
8A	VREFB8AN0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	A13	DQ3T	T_A_5	T_CA_5	
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T44n	DIFFOUT_T44n	D15	DQ3T	T_A_3	T_CA_3	
8A	VREFB8AN0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	C13	DQS3T	T_CK	T_CK	
8A	VREFB8AN0	IO			DIFFIO_TX_T46p	DIFFOUT_T46p	E17		T_A_6	T_CA_6	
8A	VREFB8AN0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	C12	DQSn3T	T_CK#	T_CK#	
8A	VREFB8AN0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	E16	DQ3T	T_A_7	T_CA_7	
8A	VREFB8AN0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	C14	DQ3T	T_BA_1		
8A	VREFB8AN0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	C16	DQ3T	T_BA_0		
8A	VREFB8AN0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	B14	DQ3T	T_BA_2		
8A	VREFB8AN0	IO			DIFFIO_TX_T48n	DIFFOUT_T48n	B15		GND	GND	
8A	VREFB8AN0	IO	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T49p	DIFFOUT_T49p	B16				
8A	VREFB8AN0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	E18	DQ4T	T_CAS#		
8A	VREFB8AN0	IO	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T49n	DIFFOUT_T49n	A15				
8A	VREFB8AN0	IO			DIFFIO_TX_T50n	DIFFOUT_T50n	D19	DQ4T	T_RAS#		
8A	VREFB8AN0	IO			DIFFIO_RX_T51p	DIFFOUT_T51p	B17	DQ4T	T_A_8	T_CA_8	
8A	VREFB8AN0	IO			DIFFIO_TX_T52p	DIFFOUT_T52p	C19	DQ4T	T_A_10		
8A	VREFB8AN0	IO			DIFFIO_RX_T51n	DIFFOUT_T51n	A17	DQ4T	T_A_9	T_CA_9	
8A	VREFB8AN0	IO			DIFFIO_TX_T52n	DIFFOUT_T52n	C18	DQ4T	T_A_11		
8A	VREFB8AN0	IO			DIFFIO_RX_T53p	DIFFOUT_T53p	A19	DQS4T	T_CS#_0	T_CS#_0	
8A	VREFB8AN0	IO			DIFFIO_TX_T54p	DIFFOUT_T54p	C21		T_A_12		
8A	VREFB8AN0	IO			DIFFIO_RX_T53n	DIFFOUT_T53n	A18	DQSn4T	T_CS#_1	T_CS#_1	
8A	VREFB8AN0	IO			DIFFIO_TX_T54n	DIFFOUT_T54n	B20	DQ4T	T_A_13		
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	B19	DQ4T	T_A_14		
8A	VREFB8AN0	IO			DIFFIO_TX_T56p	DIFFOUT_T56p	D21	DQ4T	T_WE#		
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	A20	DQ4T	T_A_15		
9A		MSEL0		MSEL0			A23				
9A		CONF_DONE		CONF_DONE			A22				
9A		MSEL1		MSEL1			A24				
9A		nSTATUS		nSTATUS			B22				
9A		nCE		nCE			A25				
9A		MSEL2		MSEL2			B25				
9A		MSEL3		MSEL3			B24				
9A		nCONFIG		nCONFIG			C23				
9A		MSEL4		MSEL4			C24				
		GND					C22				
		GND					A1				
		GND					A11				
		GND					AA1				
		GND					AA10				
		GND					AA15				
		GND					AA23				
		GND					AB13				
		GND					AB24				
		GND					AC10				
		GND					P25				GND
		GND					AC25				
		GND					AC5				
		GND					AD17				
		GND					AD22				
		GND					AE14				
		GND					AE19				
		GND					AE4				
		GND					B13				
		GND					B18				
		GND					B23				
		GND					B8				
		GND					C25				
		GND					C5				
		GND					D12				
		GND					D17				
		GND					D2				
		GND					D22				
		GND					D7				
		GND					E14				
		GND					E23				
		GND					E25				
		GND					E4				
		GND					F24				
		GND					G3				
		GND					H25				
		GND					R23				DNU
		GND					K4				
		GND					L1				
		GND					L12				
		GND					L14				
		GND					M11				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2	Board Connection Requirement for Pin Migration Only
		GND					M13				
		GND					M15				
		GND					M23				
		GND					P11				
		GND					P13				
		GND					P15				
		GND					R12				
		GND					R14				
		GND					R24				
		GND					T22				GND
		GND					T24				GND
		GND					U23				DNU
		GND					U25				GND
		GND					V23				GND
		GND					V24				GND
		GND					Y23				GND
		GND					Y25				GND
		GND					AB22				GND
		GND					F23				GND
		GND					AA24				GND
		GND					G22				GND
		GND					G24				GND
		GND					H23				GND
		GND					J23				GND
		GND					J24				GND
		GND					K22				DNU
		GND					K24				DNU
		GND					L23				GND
		GND					L25				GND
		GND					M24				GND
		GND					N22				GND
		GND					N24				GND
		GND					P23				GND
		GND					T1				
		GND					U3				
		GND					W22				
		GND					W24				
		GND					Y4				
		GND					E22				GND
		GND					F22				GND
		GND					H22				GND
		GND					J22				GND
		GND					L22				GND
		GND					M22				GND
		GND					P22				DNU
		GND					R22				GND
		GND					U22				GND
		GND					V22				GND
		GND					Y22				GND
		GND					AA22				GND
		GND					G23				DNU
		GND					H24				GND
		GND					AC24				GND
		GND					AC23				GND
		VCC					L11				
		VCC					L13				
		VCC					L15				
		VCC					M12				
		VCC					M14				
		VCC					N11				
		VCC					N12				
		VCC					N13				
		VCC					N14				
		VCC					N15				
		VCC					P12				
		VCC					P14				
		VCC					R11				
		VCC					R13				
		VCC					R15				
		VCC					K23				VCC
		VCC					T23				VCC
		VCC					N23				VCC
		VCC					P24				VCC
		VCC					W23				VCC
		VCC					Y24				VCC
		DNU					D24				
		DNU					E24				
		DNU					G2				
		DNU					B11				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2	Board Connection Requirement for Pin Migration Only
		VCCPGM					AC21				
		VCCPGM					T3				
		VCCPGM					D20				
		VCCBAT					B21				
		VCCIO3A					AB18				
		VCCIO3A					AC20				
		VCCIO3B					AC15				
		VCCIO3B					AD12				
		VCCIO3B					AE9				
		VCCIO4A					AB3				
		VCCIO4A					AB8				
		VCCIO4A					AD2				
		VCCIO4A					AD7				
		VCCIO4A					W2				
		VCCIO5A					P2				
		VCCIO5A					R4				
		VCCIO5B					J2				
		VCCIO5B					M3				
		VCCIO7A					A6				
		VCCIO7A					B3				
		VCCIO7A					C10				
		VCCIO7A					E9				
		VCCIO7A					F1				
		VCCIO8A					A16				
		VCCIO8A					A21				
		VCCIO8A					C15				
		VCCIO8A					C20				
		VCCPD3A					AB16				
		VCCPD3B4A					AB7				
		VCCPD3B4A					AC13				
		VCCPD5A					P4				
		VCCPD5B					L4				
		VCCPD7A8A					D13				
		VCCPD7A8A					D16				
		VCCPD7A8A					D6				
3A	VREFB3AN0	VREFB3AN0					AD20				
3B	VREFB3BN0	VREFB3BN0					AC11				
4A	VREFB4AN0	VREFB4AN0					AE7				
5A	VREFB5AN0	VREFB5AN0					V3				
5B	VREFB5BN0	VREFB5BN0					K3				
7A	VREFB7AN0	VREFB7AN0					C9				
8A	VREFB8AN0	VREFB8AN0					C17				
		NC					F25				DNU
		NC					G25				DNU
		NC					J25				DNU
		NC					K25				DNU
		NC					M25				DNU
		NC					N25				DNU
		NC					R25				DNU
		NC					T25				DNU
		NC					V25				DNU
		NC					W25				DNU
		NC					AA25				DNU
		NC					AB25				DNU
		RREF_TL					D25				
		VCCA_FPLL					AB23				
		VCCA_FPLL					D23				
		VCCA_FPLL					U4				
		VCCA_FPLL					G4				
		VCCA_FPLL					L24				
		VCCA_FPLL					U24				
		VCC_AUX					AA13				
		VCC_AUX					AA18				
		VCC_AUX					AB6				
		VCC_AUX					D18				
		VCC_AUX					D5				
		VCC_AUX					E12				

Notes:
(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.
(2) RESET pin is only applicable for DDR3 device.

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
3A		TDO		TDO			M5				
3A		nCSO		DATA4			R4				
3A		TMS		TMS			P5				
3A		AS_DATA3		DATA3			T4				
3A		TCK		TCK			V5				
3A		AS_DATA2		DATA2			AA5				
3A		TDI		TDI			W5				
3A		AS_DATA1		DATA1			AB3				
3A		DCLK		DCLK			V3				
3A		AS_DATA0,ASDO		DATA0			AB4				
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	R6	DQ1B			
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	U7				
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	R5	DQ1B			
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	U8	DQ1B			
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	P6	DQSn1B			
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	W8	DQ1B			
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	N6	DQS1B			
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	W9				
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	T7	DQ1B			
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	U6	DQ1B			
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	T8	DQ1B			
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	V6	DQ1B			
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	M6				
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	R7	DQ1B			
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	M7				
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	P7	DQ1B			
3B	VREFB3BN0	IO			DIFFIO_TX_B9n	DIFFOUT_B9n	AB6			GND	GND
3B	VREFB3BN0	IO			DIFFIO_RX_B10n	DIFFOUT_B10n	V9	DQ2B		B_A_15	
3B	VREFB3BN0	IO			DIFFIO_TX_B9p	DIFFOUT_B9p	AB5	DQ2B		B_WE#	
3B	VREFB3BN0	IO			DIFFIO_RX_B10p	DIFFOUT_B10p	V10	DQ2B		B_A_14	
3B	VREFB3BN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	P8	DQSn2B		B_CS#_1	B_CS#_1
3B	VREFB3BN0	IO			DIFFIO_TX_B12n	DIFFOUT_B12n	AA7	DQ2B		B_A_13	
3B	VREFB3BN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	N8	DQS2B		B_CS#_0	B_CS#_0
3B	VREFB3BN0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AB7			B_A_12	
3B	VREFB3BN0	IO			DIFFIO_TX_B13n	DIFFOUT_B13n	AA8	DQ2B		B_A_11	
3B	VREFB3BN0	IO			DIFFIO_RX_B14n	DIFFOUT_B14n	T9	DQ2B		B_A_9	B_CA_9
3B	VREFB3BN0	IO			DIFFIO_TX_B13p	DIFFOUT_B13p	AB8	DQ2B		B_A_10	
3B	VREFB3BN0	IO			DIFFIO_RX_B14p	DIFFOUT_B14p	U10	DQ2B		B_A_8	B_CA_8
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B15n	DIFFOUT_B15n	M8				
3B	VREFB3BN0	IO			DIFFIO_TX_B16n	DIFFOUT_B16n	AA10	DQ2B		B_RAS#	
3B	VREFB3BN0	IO	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B15p	DIFFOUT_B15p	M9				
3B	VREFB3BN0	IO			DIFFIO_TX_B16p	DIFFOUT_B16p	AA9	DQ2B		B_CAS#	
3B	VREFB3BN0	IO			DIFFIO_TX_B17n	DIFFOUT_B17n	Y10			GND	GND
3B	VREFB3BN0	IO			DIFFIO_RX_B18n	DIFFOUT_B18n	T10	DQ3B		B_BA_2	
3B	VREFB3BN0	IO			DIFFIO_TX_B17p	DIFFOUT_B17p	Y9	DQ3B		B_BA_0	
3B	VREFB3BN0	IO			DIFFIO_RX_B18p	DIFFOUT_B18p	R9	DQ3B		B_BA_1	
3B	VREFB3BN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	U11	DQSn3B		B_CK#	B_CK#
3B	VREFB3BN0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	R12	DQ3B		B_A_7	B_CA_7
3B	VREFB3BN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	U12	DQS3B		B_CK	B_CK
3B	VREFB3BN0	IO			DIFFIO_TX_B20p	DIFFOUT_B20p	P12			B_A_6	B_CA_6
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B21n	DIFFOUT_B21n	AB10	DQ3B		B_A_3	B_CA_3
3B	VREFB3BN0	IO			DIFFIO_RX_B22n	DIFFOUT_B22n	R10	DQ3B		B_A_5	B_CA_5
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p	DIFFOUT_B21p	AB11	DQ3B		B_A_2	B_CA_2
3B	VREFB3BN0	IO			DIFFIO_RX_B22p	DIFFOUT_B22p	R11	DQ3B		B_A_4	B_CA_4
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B23n	DIFFOUT_B23n	P9				
3B	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	Y11	DQ3B		B_A_1	B_CA_1
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B23p	DIFFOUT_B23p	N9				
3B	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	AA12	DQ3B		B_A_0	B_CA_0
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B25n	DIFFOUT_B25n	AB13				
4A	VREFB4AN0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	V13	DQ4B		B_DQ_0	B_DQ_0
4A	VREFB4AN0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	AB12	DQ4B		B_DQ_2	B_DQ_2
4A	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	U13	DQ4B		B_DQ_1	B_DQ_1
4A	VREFB4AN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	T12	DQSn4B		B_DQS#_0	B_DQS#_0
4A	VREFB4AN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AA14	DQ4B		B_DQ_3	B_DQ_3
4A	VREFB4AN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	T13	DQS4B		B_DQS_0	B_DQS_0
4A	VREFB4AN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AA13			B_ODT_0	B_ODT_0
4A	VREFB4AN0	IO			DIFFIO_TX_B29n	DIFFOUT_B29n	AB15	DQ4B		B_ODT_1	B_ODT_1
4A	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	Y14	DQ4B		B_DQ_4	B_DQ_4
4A	VREFB4AN0	IO			DIFFIO_TX_B29p	DIFFOUT_B29p	AA15	DQ4B		B_DQ_6	B_DQ_6
4A	VREFB4AN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	Y15	DQ4B		B_DQ_5	B_DQ_5
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B31n	DIFFOUT_B31n	V14				
4A	VREFB4AN0	IO			DIFFIO_TX_B32n	DIFFOUT_B32n	AB17	DQ4B		B_DQ_7	B_DQ_7

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B31p	DIFFOUT_B31p	V15				
4A	VREFB4AN0	IO			DIFFIO_TX_B32p	DIFFOUT_B32p	AB18	DQ4B		B_DM_0	B_DM_0
4A	VREFB4AN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AB20			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	Y16	DQ5B	DQ1B	B_DQ_8	B_DQ_8
4A	VREFB4AN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AB21	DQ5B	DQ1B	B_DQ_10	B_DQ_10
4A	VREFB4AN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	Y17	DQ5B	DQ1B	B_DQ_9	B_DQ_9
4A	VREFB4AN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	T14	DQSn5B	DQ1B	B_DQS#_1	B_DQS#_1
4A	VREFB4AN0	IO			DIFFIO_TX_B36n	DIFFOUT_B36n	AA17	DQ5B	DQ1B	B_DQ_11	B_DQ_11
4A	VREFB4AN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	U15	DQS5B	DQ1B	B_DQS_1	B_DQS_1
4A	VREFB4AN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	AA18			B_CKE_1	B_CKE_1
4A	VREFB4AN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AA19	DQ5B	DQ1B	B_CKE_0	B_CKE_0
4A	VREFB4AN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	V20	DQ5B	DQ1B	B_DQ_12	B_DQ_12
4A	VREFB4AN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	AA20	DQ5B	DQ1B	B_DQ_14	B_DQ_14
4A	VREFB4AN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	W19	DQ5B	DQ1B	B_DQ_13	B_DQ_13
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B39n	DIFFOUT_B39n	V16				
4A	VREFB4AN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	AB22	DQ5B	DQ1B	B_DQ_15	B_DQ_15
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B39p	DIFFOUT_B39p	W16				
4A	VREFB4AN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	AA22	DQ5B	DQ1B	B_DM_1	B_DM_1
4A	VREFB4AN0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	Y22			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	Y20	DQ6B	DQ1B	B_DQ_16	B_DQ_16
4A	VREFB4AN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	W22	DQ6B	DQ1B	B_DQ_18	B_DQ_18
4A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	Y19	DQ6B	DQ1B	B_DQ_17	B_DQ_17
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	P14	DQSn6B	DQSn1B	B_DQS#_2	B_DQS#_2
4A	VREFB4AN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	Y21	DQ6B	DQ1B	B_DQ_19	B_DQ_19
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	R14	DQS6B	DQS1B	B_DQS_2	B_DQS_2
4A	VREFB4AN0	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	W21			B_RESET#	B_RESET#
4A	VREFB4AN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	U22	DQ6B	DQ1B	GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	V19	DQ6B	DQ1B	B_DQ_20	B_DQ_20
4A	VREFB4AN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	V21	DQ6B	DQ1B	B_DQ_22	B_DQ_22
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	V18	DQ6B	DQ1B	B_DQ_21	B_DQ_21
4A	VREFB4AN0	IO			DIFFIO_RX_B47n	DIFFOUT_B47n	U16			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	U21	DQ6B	DQ1B	B_DQ_23	B_DQ_23
4A	VREFB4AN0	IO			DIFFIO_RX_B47p	DIFFOUT_B47p	U17			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	U20	DQ6B	DQ1B	B_DM_2	B_DM_2
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	T19	DQ1R			
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	T18				
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	T20	DQ1R			
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	T17				
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	T22	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	T15	DQ1R			
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	R22	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	R15	DQ1R			
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	R21				
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	R16	DQS1R			
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	P22	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	R17	DQSn1R			
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	P19	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	P16	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	P18				
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	P17	DQ1R			
5B	VREFB5BN0	IO	CLK6p		DIFFIO_RX_R17p	DIFFOUT_R17p	N16				
5B	VREFB5BN0	IO			DIFFIO_TX_R18p	DIFFOUT_R18p	N20	DQ2R			
5B	VREFB5BN0	IO	CLK6n		DIFFIO_RX_R17n	DIFFOUT_R17n	M16				
5B	VREFB5BN0	IO			DIFFIO_TX_R18n	DIFFOUT_R18n	N21	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	N19	DQ2R			
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R20p	DIFFOUT_R20p	M22	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R19n	DIFFOUT_R19n	M18	DQ2R			
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R20n	DIFFOUT_R20n	L22	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R21p	DIFFOUT_R21p	K17	DQS2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R22p	DIFFOUT_R22p	M20				
5B	VREFB5BN0	IO			DIFFIO_RX_R21n	DIFFOUT_R21n	L17	DQSn2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R22n	DIFFOUT_R22n	M21	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R23p	DIFFOUT_R23p	L19	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R24p	DIFFOUT_R24p	K21	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	L18	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R24n	DIFFOUT_R24n	K22				
7A		GND					F17				
7A	VREFB7AN0	IO			DIFFIO_RX_T1p	DIFFOUT_T1p	H21			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T2p	DIFFOUT_T2p	E21	DQ1T	DQ1T	T_DM_4	T_DM_4
7A	VREFB7AN0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	G21			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T2n	DIFFOUT_T2n	D21	DQ1T	DQ1T	T_DQ_39	T_DQ_39
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T3p	E19	DQ1T	DQ1T	T_DQ_37	T_DQ_37

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
7A	VREFB7AN0	IO			DIFFIO_TX_T4p	DIFFOUT_T4p	C20	DQ1T	DQ1T	T_DQ_38	T_DQ_38
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T3n	D19	DQ1T	DQ1T	T_DQ_36	T_DQ_36
7A	VREFB7AN0	IO			DIFFIO_TX_T4n	DIFFOUT_T4n	B20	DQ1T	DQ1T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T5p	J21	DQS1T	DQS1T	T_DQS_4	T_DQS_4
7A	VREFB7AN0	IO			DIFFIO_TX_T6p	DIFFOUT_T6p	B18			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T5n	J22	DQSn1T	DQSn1T	T_DQS#_4	T_DQS#_4
7A	VREFB7AN0	IO			DIFFIO_TX_T6n	DIFFOUT_T6n	B17	DQ1T	DQ1T	T_DQ_35	T_DQ_35
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T7p	C21	DQ1T	DQ1T	T_DQ_33	T_DQ_33
7A	VREFB7AN0	IO			DIFFIO_TX_T8p	DIFFOUT_T8p	G22	DQ1T	DQ1T	T_DQ_34	T_DQ_34
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T7n	B21	DQ1T	DQ1T	T_DQ_32	T_DQ_32
7A	VREFB7AN0	IO			DIFFIO_TX_T8n	DIFFOUT_T8n	F22			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T9p	G20			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T10p	DIFFOUT_T10p	E22	DQ2T	DQ1T	T_DM_3	T_DM_3
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T9n	H20			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T10n	DIFFOUT_T10n	D22	DQ2T	DQ1T	T_DQ_31	T_DQ_31
7A	VREFB7AN0	IO			DIFFIO_RX_T11p	DIFFOUT_T11p	C19	DQ2T	DQ1T	T_DQ_29	T_DQ_29
7A	VREFB7AN0	IO			DIFFIO_TX_T12p	DIFFOUT_T12p	B22	DQ2T	DQ1T	T_DQ_30	T_DQ_30
7A	VREFB7AN0	IO			DIFFIO_RX_T11n	DIFFOUT_T11n	C18	DQ2T	DQ1T	T_DQ_28	T_DQ_28
7A	VREFB7AN0	IO			DIFFIO_TX_T12n	DIFFOUT_T12n	A22	DQ2T	DQ1T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T13p	DIFFOUT_T13p	F19	DQS2T	DQ1T	T_DQS_3	T_DQS_3
7A	VREFB7AN0	IO			DIFFIO_TX_T14p	DIFFOUT_T14p	E20			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T13n	DIFFOUT_T13n	F18	DQSn2T	DQ1T	T_DQS#_3	T_DQS#_3
7A	VREFB7AN0	IO			DIFFIO_TX_T14n	DIFFOUT_T14n	F20	DQ2T	DQ1T	T_DQ_27	T_DQ_27
7A	VREFB7AN0	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	A18	DQ2T	DQ1T	T_DQ_25	T_DQ_25
7A	VREFB7AN0	IO			DIFFIO_TX_T16p	DIFFOUT_T16p	A20	DQ2T	DQ1T	T_DQ_26	T_DQ_26
7A	VREFB7AN0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	A17	DQ2T	DQ1T	T_DQ_24	T_DQ_24
7A	VREFB7AN0	IO			DIFFIO_TX_T16n	DIFFOUT_T16n	A19			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	K20			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	B16	DQ3T	DQ2T	T_DM_2	T_DM_2
7A	VREFB7AN0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	K19			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T18n	DIFFOUT_T18n	C16	DQ3T	DQ2T	T_DQ_23	T_DQ_23
7A	VREFB7AN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	D17	DQ3T	DQ2T	T_DQ_21	T_DQ_21
7A	VREFB7AN0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	G17	DQ3T	DQ2T	T_DQ_22	T_DQ_22
7A	VREFB7AN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	E16	DQ3T	DQ2T	T_DQ_20	T_DQ_20
7A	VREFB7AN0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	G16	DQ3T	DQ2T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	G18	DQS3T	DQS2T	T_DQS_2	T_DQS_2
7A	VREFB7AN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	J19			T_RESET#	T_RESET#
7A	VREFB7AN0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	H18	DQSn3T	DQSn2T	T_DQS#_2	T_DQS#_2
7A	VREFB7AN0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	J18	DQ3T	DQ2T	T_DQ_19	T_DQ_19
7A	VREFB7AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	E15	DQ3T	DQ2T	T_DQ_17	T_DQ_17
7A	VREFB7AN0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	A15	DQ3T	DQ2T	T_DQ_18	T_DQ_18
7A	VREFB7AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	F15	DQ3T	DQ2T	T_DQ_16	T_DQ_16
7A	VREFB7AN0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	A14			GND	GND
7A	VREFB7AN0	IO	CLK11p		DIFFIO_RX_T25p	DIFFOUT_T25p	H16				
7A	VREFB7AN0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	J17	DQ4T	DQ2T	T_DM_1	T_DM_1
7A	VREFB7AN0	IO	CLK11n		DIFFIO_RX_T25n	DIFFOUT_T25n	H15				
7A	VREFB7AN0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	K16	DQ4T	DQ2T	T_DQ_15	T_DQ_15
7A	VREFB7AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	C15	DQ4T	DQ2T	T_DQ_13	T_DQ_13
7A	VREFB7AN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	G15	DQ4T	DQ2T	T_DQ_14	T_DQ_14
7A	VREFB7AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	B15	DQ4T	DQ2T	T_DQ_12	T_DQ_12
7A	VREFB7AN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	F14	DQ4T	DQ2T	T_CKE_0	T_CKE_0
7A	VREFB7AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	H14	DQS4T	DQ2T	T_DQS_1	T_DQS_1
7A	VREFB7AN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	B13			T_CKE_1	T_CKE_1
7A	VREFB7AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	J13	DQSn4T	DQ2T	T_DQS#_1	T_DQS#_1
7A	VREFB7AN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	A13	DQ4T	DQ2T	T_DQ_11	T_DQ_11
7A	VREFB7AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	E14	DQ4T	DQ2T	T_DQ_9	T_DQ_9
7A	VREFB7AN0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	J11	DQ4T	DQ2T	T_DQ_10	T_DQ_10
7A	VREFB7AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	F13	DQ4T	DQ2T	T_DQ_8	T_DQ_8
7A	VREFB7AN0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	H10			GND	GND
7A	VREFB7AN0	IO	CLK10p		DIFFIO_RX_T33p	DIFFOUT_T33p	H13				
7A	VREFB7AN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	G11	DQ5T		T_DM_0	T_DM_0
7A	VREFB7AN0	IO	CLK10n		DIFFIO_RX_T33n	DIFFOUT_T33n	G13				
7A	VREFB7AN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	F12	DQ5T		T_DQ_7	T_DQ_7
7A	VREFB7AN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	D13	DQ5T		T_DQ_5	T_DQ_5
7A	VREFB7AN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	B12	DQ5T		T_DQ_6	T_DQ_6
7A	VREFB7AN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	C13	DQ5T		T_DQ_4	T_DQ_4
7A	VREFB7AN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	A12	DQ5T		T_ODT_1	T_ODT_1
7A	VREFB7AN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	H11	DQS5T		T_DQS_0	T_DQS_0
7A	VREFB7AN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	L8			T_ODT_0	T_ODT_0
7A	VREFB7AN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	G12	DQSn5T		T_DQS#_0	T_DQS#_0
7A	VREFB7AN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	K9	DQ5T		T_DQ_3	T_DQ_3
7A	VREFB7AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	D12	DQ5T		T_DQ_1	T_DQ_1

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
7A	VREFB7AN0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	C11	DQ5T		T_DQ_2	T_DQ_2
7A	VREFB7AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	E12	DQ5T		T_DQ_0	T_DQ_0
7A	VREFB7AN0	IO	RZQ_2		DIFFIO_TX_T40n	DIFFOUT_T40n	B11				
8A	VREFB8AN0	IO	CLK9p		DIFFIO_RX_T41p	DIFFOUT_T41p	G10				
8A	VREFB8AN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	L7	DQ6T		T_A_0	T_CA_0
8A	VREFB8AN0	IO	CLK9n		DIFFIO_RX_T41n	DIFFOUT_T41n	F10				
8A	VREFB8AN0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	K7	DQ6T		T_A_1	T_CA_1
8A	VREFB8AN0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	J7	DQ6T		T_A_4	T_CA_4
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T44p	DIFFOUT_T44p	H8	DQ6T		T_A_2	T_CA_2
8A	VREFB8AN0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	J8	DQ6T		T_A_5	T_CA_5
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T44n	DIFFOUT_T44n	G8	DQ6T		T_A_3	T_CA_3
8A	VREFB8AN0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	J9	DQS6T		T_CK	T_CK
8A	VREFB8AN0	IO			DIFFIO_TX_T46p	DIFFOUT_T46p	A10			T_A_6	T_CA_6
8A	VREFB8AN0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	H9	DQSn6T		T_CK#	T_CK#
8A	VREFB8AN0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	A9	DQ6T		T_A_7	T_CA_7
8A	VREFB8AN0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	B10	DQ6T		T_BA_1	
8A	VREFB8AN0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	A5	DQ6T		T_BA_0	
8A	VREFB8AN0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	C9	DQ6T		T_BA_2	
8A	VREFB8AN0	IO			DIFFIO_TX_T48n	DIFFOUT_T48n	B5			GND	GND
8A	VREFB8AN0	IO	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T49p	DIFFOUT_T49p	E10				
8A	VREFB8AN0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	B6	DQ7T		T_CAS#	
8A	VREFB8AN0	IO	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T49n	DIFFOUT_T49n	F9				
8A	VREFB8AN0	IO			DIFFIO_TX_T50n	DIFFOUT_T50n	B7	DQ7T		T_RAS#	
8A	VREFB8AN0	IO			DIFFIO_RX_T51p	DIFFOUT_T51p	A8	DQ7T		T_A_8	T_CA_8
8A	VREFB8AN0	IO			DIFFIO_TX_T52p	DIFFOUT_T52p	C6	DQ7T		T_A_10	
8A	VREFB8AN0	IO			DIFFIO_RX_T51n	DIFFOUT_T51n	A7	DQ7T		T_A_9	T_CA_9
8A	VREFB8AN0	IO			DIFFIO_TX_T52n	DIFFOUT_T52n	D6	DQ7T		T_A_11	
8A	VREFB8AN0	IO			DIFFIO_RX_T53p	DIFFOUT_T53p	E9	DQS7T		T_CS#_0	T_CS#_0
8A	VREFB8AN0	IO			DIFFIO_TX_T54p	DIFFOUT_T54p	D7			T_A_12	
8A	VREFB8AN0	IO			DIFFIO_RX_T53n	DIFFOUT_T53n	D9	DQSn7T		T_CS#_1	T_CS#_1
8A	VREFB8AN0	IO			DIFFIO_TX_T54n	DIFFOUT_T54n	C8	DQ7T		T_A_13	
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	G6	DQ7T		T_A_14	
8A	VREFB8AN0	IO			DIFFIO_TX_T56p	DIFFOUT_T56p	F7	DQ7T		T_WE#	
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	H6	DQ7T		T_A_15	
8A	VREFB8AN0	IO			DIFFIO_TX_T56n	DIFFOUT_T56n	E7			GND	GND
9A		MSEL0		MSEL0			L6				
9A		CONF_DONE		CONF_DONE			K6				
9A		MSEL1		MSEL1			J6				
9A		nSTATUS		nSTATUS			H5				
9A		nCE		nCE			G5				
9A		MSEL2		MSEL2			A2				
9A		MSEL3		MSEL3			E5				
9A		nCONFIG		nCONFIG			A4				
9A		MSEL4		MSEL4			F3				
9A		GND					C5				
		GND					F5				
		GND					G4				
		GND					V4				
		GND					U4				
		GND					AB19				
		GND					AB14				
		GND					AB9				
		GND					AB2				
		GND					AB1				
		GND					AA11				
		GND					AA6				
		GND					AA4				
		GND					AA3				
		GND					Y18				
		GND					Y5				
		GND					Y2				
		GND					Y1				
		GND					W4				
		GND					W3				
		GND					V22				
		GND					V17				
		GND					V12				
		GND					V7				
		GND					V2				
		GND					V1				
		GND					U9				
		GND					U5				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		GND					U3				
		GND					T21				
		GND					T16				
		GND					T2				
		GND					T1				
		GND					R13				
		GND					R3				
		GND					P10				
		GND					P4				
		GND					P2				
		GND					P1				
		GND					N22				
		GND					N17				
		GND					N15				
		GND					N13				
		GND					N11				
		GND					N7				
		GND					N5				
		GND					N3				
		GND					M14				
		GND					M12				
		GND					M10				
		GND					M4				
		GND					M2				
		GND					M1				
		GND					L21				
		GND					L15				
		GND					L13				
		GND					L11				
		GND					L5				
		GND					L3				
		GND					K14				
		GND					K12				
		GND					K10				
		GND					K8				
		GND					K4				
		GND					K2				
		GND					K1				
		GND					J20				
		GND					J15				
		GND					J5				
		GND					J3				
		GND					H22				
		GND					H12				
		GND					H7				
		GND					H4				
		GND					H3				
		GND					H2				
		GND					H1				
		GND					G19				
		GND					G9				
		GND					G3				
		GND					F16				
		GND					F6				
		GND					F2				
		GND					F1				
		GND					E13				
		GND					E4				
		GND					E3				
		GND					D20				
		GND					D10				
		GND					D5				
		GND					D2				
		GND					D1				
		GND					C17				
		GND					C4				
		GND					C3				
		GND					B14				
		GND					B9				
		GND					B2				
		GND					B1				
		GND					A21				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		GND					A11				
		VCC					P15				
		VCC					P13				
		VCC					P11				
		VCC					N14				
		VCC					N12				
		VCC					N10				
		VCC					M15				
		VCC					M13				
		VCC					M11				
		VCC					L16				
		VCC					L14				
		VCC					L12				
		VCC					L10				
		VCC					K15				
		VCC					K13				
		VCC					K11				
		VCC					J16				
		VCC					J14				
		VCC					J12				
		VCC					J10				
		VCC					P3				
		VCC					K3				
		VCC					L4				
		VCC					N4				
		VCC					K5				
		VCC					J4				
		DNU					B3				
		DNU					B4				
		DNU					E17				
		DNU					L9				
		VCCPGM					V8				
		VCCPGM					R19				
		VCCPGM					F8				
		VCCBAT					A3				
		VCCIO3A					T6				
		VCCIO3A					Y8				
		VCCIO3B					Y13				
		VCCIO3B					W10				
		VCCIO3B					T11				
		VCCIO3B					R8				
		VCCIO4A					U19				
		VCCIO4A					AA21				
		VCCIO4A					AA16				
		VCCIO4A					W20				
		VCCIO4A					W15				
		VCCIO4A					U14				
		VCCIO5A					R18				
		VCCIO5A					P20				
		VCCIO5B					M19				
		VCCIO5B					K18				
		VCCIO7A					B19				
		VCCIO7A					H17				
		VCCIO7A					G14				
		VCCIO7A					F21				
		VCCIO7A					F11				
		VCCIO7A					E18				
		VCCIO7A					D15				
		VCCIO7A					C22				
		VCCIO7A					C12				
		VCCIO7A					A16				
		VCCIO8A					A6				
		VCCIO8A					G7				
		VCCIO8A					E8				
		VCCIO8A					C7				
		VCCPD3A					W6				
		VCCPD3B4A					W17				
		VCCPD3B4A					W14				
		VCCPD3B4A					W12				
		VCCPD3B4A					W11				
		VCCPD5A					P21				
		VCCPD5B					N18				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		VCCPD5B					M17				
		VCCPD7A8A					E11				
		VCCPD7A8A					D16				
		VCCPD7A8A					D14				
		VCCPD7A8A					D8				
		VCCPD7A8A					C10				
3A	VREFB3AN0	VREFB3AN0					Y7				
3B	VREFB3BN0	VREFB3BN0					Y12				
4A	VREFB4AN0	VREFB4AN0					AB16				
5A	VREFB5AN0	VREFB5AN0					R20				
5B	VREFB5BN0	VREFB5BN0					L20				
7A	VREFB7AN0	VREFB7AN0					C14				
8A	VREFB8AN0	VREFB8AN0					B8				
		NC					Y6				
		NC					V11				
		NC					C2				
		NC					C1				
		NC					G2				
		NC					G1				
		NC					L2				
		NC					L1				
		NC					R2				
		NC					R1				
		NC					W2				
		NC					W1				
		NC					AA2				
		NC					AA1				
		NC					D3				
		NC					D4				
		NC					E1				
		NC					E2				
		NC					J1				
		NC					J2				
		NC					N1				
		NC					N2				
		NC					U1				
		NC					U2				
		NC					Y3				
		NC					Y4				
		RREF_TL					A1				
		VCCA_FPLL					T5				
		VCCA_FPLL					F4				
		VCCA_FPLL					U18				
		VCCA_FPLL					H19				
		VCCA_FPLL					M3				
		VCCA_FPLL					T3				
		VCC_AUX					E6				
		VCC_AUX					D18				
		VCC_AUX					W18				
		VCC_AUX					W13				
		VCC_AUX					W7				
		VCC_AUX					D11				

Notes:
(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.
(2) RESET pin is only applicable for DDR3 device.

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
3A		TDO		TDO			V3				
3A		nCSO		DATA4			AB6				
3A		TMS		TMS			R4				
3A		AS_DATA3		DATA3			AA5				
3A		TCK		TCK			V5				
3A		AS_DATA2		DATA2			T5				
3A		TDI		TDI			P5				
3A		AS_DATA1		DATA1			W5				
3A		DCLK		DCLK			M5				
3A		AS_DATA0,ASDO		DATA0			AB4				
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	P6	DQ1B			
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	U7				
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	N6	DQ1B			
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	U6	DQ1B			
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	M6	DQSn1B			
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	R5	DQ1B			
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	M7	DQS1B			
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	R6				
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	R7	DQ1B			
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	L7	DQ1B			
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	T7	DQ1B			
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	L8	DQ1B			
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	T8				
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	P7	DQ1B			
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	T9				
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	P8	DQ1B			
3B	VREFB3BN0	IO			DIFFIO_TX_B9n	DIFFOUT_B9n	V8			GND	GND
3B	VREFB3BN0	IO			DIFFIO_RX_B10n	DIFFOUT_B10n	N8	DQ2B		B_A_15	
3B	VREFB3BN0	IO			DIFFIO_TX_B9p	DIFFOUT_B9p	W8	DQ2B		B_WE#	
3B	VREFB3BN0	IO			DIFFIO_RX_B10p	DIFFOUT_B10p	M8	DQ2B		B_A_14	
3B	VREFB3BN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	N9	DQSn2B		B_CS#_1	B_CS#_1
3B	VREFB3BN0	IO			DIFFIO_TX_B12n	DIFFOUT_B12n	AA7	DQ2B		B_A_13	
3B	VREFB3BN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	N10	DQS2B		B_CS#_0	B_CS#_0
3B	VREFB3BN0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AB7			B_A_12	
3B	VREFB3BN0	IO			DIFFIO_TX_B13n	DIFFOUT_B13n	Y7	DQ2B		B_A_11	
3B	VREFB3BN0	IO			DIFFIO_RX_B14n	DIFFOUT_B14n	U8	DQ2B		B_A_9	B_CA_9
3B	VREFB3BN0	IO			DIFFIO_TX_B13p	DIFFOUT_B13p	W7	DQ2B		B_A_10	
3B	VREFB3BN0	IO			DIFFIO_RX_B14p	DIFFOUT_B14p	V9	DQ2B		B_A_8	B_CA_8
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B15n	DIFFOUT_B15n	R9				
3B	VREFB3BN0	IO			DIFFIO_TX_B16n	DIFFOUT_B16n	AB8	DQ2B		B_RAS#	
3B	VREFB3BN0	IO	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B15p	DIFFOUT_B15p	P9				
3B	VREFB3BN0	IO			DIFFIO_TX_B16p	DIFFOUT_B16p	AA8	DQ2B		B_CAS#	
3B	VREFB3BN0	IO			DIFFIO_TX_B17n	DIFFOUT_B17n	Y10			GND	GND
3B	VREFB3BN0	IO			DIFFIO_RX_B18n	DIFFOUT_B18n	AA9	DQ3B		B_BA_2	
3B	VREFB3BN0	IO			DIFFIO_TX_B17p	DIFFOUT_B17p	AA10	DQ3B		B_BA_0	
3B	VREFB3BN0	IO			DIFFIO_RX_B18p	DIFFOUT_B18p	Y9	DQ3B		B_BA_1	
3B	VREFB3BN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	L9	DQSn3B		B_CK#	B_CK#
3B	VREFB3BN0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	W11	DQ3B		B_A_7	B_CA_7
3B	VREFB3BN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	M10	DQS3B		B_CK	B_CK
3B	VREFB3BN0	IO			DIFFIO_TX_B20p	DIFFOUT_B20p	Y11			B_A_6	B_CA_6
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B21n	DIFFOUT_B21n	AB10	DQ3B		B_A_3	B_CA_3
3B	VREFB3BN0	IO			DIFFIO_RX_B22n	DIFFOUT_B22n	U10	DQ3B		B_A_5	B_CA_5
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p	DIFFOUT_B21p	AB11	DQ3B		B_A_2	B_CA_2
3B	VREFB3BN0	IO			DIFFIO_RX_B22p	DIFFOUT_B22p	U11	DQ3B		B_A_4	B_CA_4
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B23n	DIFFOUT_B23n	T10				
3B	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	R11	DQ3B		B_A_1	B_CA_1
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B23p	DIFFOUT_B23p	R10				
3B	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	P12	DQ3B		B_A_0	B_CA_0
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B25n	DIFFOUT_B25n	AA13				
4A	VREFB4AN0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	W12	DQ4B		B_DQ_0	B_DQ_0
4A	VREFB4AN0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	AB13	DQ4B		B_DQ_2	B_DQ_2
4A	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	Y12	DQ4B		B_DQ_1	B_DQ_1
4A	VREFB4AN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	U12	DQSn4B		B_DQS#_0	B_DQS#_0
4A	VREFB4AN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	R12	DQ4B		B_DQ_3	B_DQ_3
4A	VREFB4AN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	T12	DQS4B		B_DQS_0	B_DQS_0
4A	VREFB4AN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	T13			B_ODT_0	B_ODT_0
4A	VREFB4AN0	IO			DIFFIO_TX_B29n	DIFFOUT_B29n	AB15	DQ4B		B_ODT_1	B_ODT_1
4A	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	W13	DQ4B		B_DQ_4	B_DQ_4
4A	VREFB4AN0	IO			DIFFIO_TX_B29p	DIFFOUT_B29p	AB16	DQ4B		B_DQ_6	B_DQ_6
4A	VREFB4AN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	V13	DQ4B		B_DQ_5	B_DQ_5
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B31n	DIFFOUT_B31n	T14				
4A	VREFB4AN0	IO			DIFFIO_TX_B32n	DIFFOUT_B32n	AB18	DQ4B		B_DQ_7	B_DQ_7

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B31p	DIFFOUT_B31p	U13				
4A	VREFB4AN0	IO			DIFFIO_TX_B32p	DIFFOUT_B32p	AA18	DQ4B		B_DM_0	B_DM_0
4A	VREFB4AN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AA19			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	Y14	DQ5B	DQ1B	B_DQ_8	B_DQ_8
4A	VREFB4AN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	Y19	DQ5B	DQ1B	B_DQ_10	B_DQ_10
4A	VREFB4AN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	W14	DQ5B	DQ1B	B_DQ_9	B_DQ_9
4A	VREFB4AN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	P14	DQSn5B	DQ1B	B_DQS#_1	B_DQS#_1
4A	VREFB4AN0	IO			DIFFIO_TX_B36n	DIFFOUT_B36n	AA20	DQ5B	DQ1B	B_DQ_11	B_DQ_11
4A	VREFB4AN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	R14	DQS5B	DQ1B	B_DQS_1	B_DQS_1
4A	VREFB4AN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	Y20			B_CKE_1	B_CKE_1
4A	VREFB4AN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AA15	DQ5B	DQ1B	B_CKE_0	B_CKE_0
4A	VREFB4AN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	U15	DQ5B	DQ1B	B_DQ_12	B_DQ_12
4A	VREFB4AN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	Y15	DQ5B	DQ1B	B_DQ_14	B_DQ_14
4A	VREFB4AN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	V15	DQ5B	DQ1B	B_DQ_13	B_DQ_13
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B39n	DIFFOUT_B39n	R15				
4A	VREFB4AN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	AB20	DQ5B	DQ1B	B_DQ_15	B_DQ_15
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B39p	DIFFOUT_B39p	T15				
4A	VREFB4AN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	AB21	DQ5B	DQ1B	B_DM_1	B_DM_1
4A	VREFB4AN0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	AB22			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	Y16	DQ6B	DQ1B	B_DQ_16	B_DQ_16
4A	VREFB4AN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AA22	DQ6B	DQ1B	B_DQ_18	B_DQ_18
4A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	Y17	DQ6B	DQ1B	B_DQ_17	B_DQ_17
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	U16	DQSn6B	DQSn1B	B_DQS#_2	B_DQS#_2
4A	VREFB4AN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	AA17	DQ6B	DQ1B	B_DQ_19	B_DQ_19
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	U17	DQS6B	DQS1B	B_DQS_2	B_DQS_2
4A	VREFB4AN0	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	AB17			B_RESET#	B_RESET#
4A	VREFB4AN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	Y22	DQ6B	DQ1B	GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	V18	DQ6B	DQ1B	B_DQ_20	B_DQ_20
4A	VREFB4AN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	Y21	DQ6B	DQ1B	B_DQ_22	B_DQ_22
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	W18	DQ6B	DQ1B	B_DQ_21	B_DQ_21
4A	VREFB4AN0	IO			DIFFIO_RX_B47n	DIFFOUT_B47n	W16			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	W21	DQ6B	DQ1B	B_DQ_23	B_DQ_23
4A	VREFB4AN0	IO			DIFFIO_RX_B47p	DIFFOUT_B47p	W17			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	W22	DQ6B	DQ1B	B_DM_2	B_DM_2
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	U22	DQ1R			
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	V20				
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	U21	DQ1R			
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	V19				
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	T19	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	T17	DQ1R			
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	T20	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	T18	DQ1R			
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	T22				
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	R16	DQS1R			
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	R22	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	R17	DQSn1R			
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	R20	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	R19	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	R21				
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	P19	DQ1R			
5B	VREFB5BN0	IO	CLK7p,FPLL_BR_FBp		DIFFIO_RX_R9p	DIFFOUT_R9p	M16				
5B	VREFB5BN0	IO			DIFFIO_TX_R10p	DIFFOUT_R10p	E21	DQ2R			
5B	VREFB5BN0	IO	CLK7n,FPLL_BR_FBn		DIFFIO_RX_R9n	DIFFOUT_R9n	M17				
5B	VREFB5BN0	IO			DIFFIO_TX_R10n	DIFFOUT_R10n	D22	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	L19	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R12p	DIFFOUT_R12p	K21	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	L20	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R12n	DIFFOUT_R12n	J21	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R13p	DIFFOUT_R13p	L15	DQS2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R14p	DIFFOUT_R14p	G22				
5B	VREFB5BN0	IO			DIFFIO_RX_R13n	DIFFOUT_R13n	K15	DQSn2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R14n	DIFFOUT_R14n	G21	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R15p	DIFFOUT_R15p	L18	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R16p	DIFFOUT_R16p	G20	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R15n	DIFFOUT_R15n	K19	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R16n	DIFFOUT_R16n	H21				
5B	VREFB5BN0	IO	CLK6p		DIFFIO_RX_R17p	DIFFOUT_R17p	L17				
5B	VREFB5BN0	IO			DIFFIO_TX_R18p	DIFFOUT_R18p	E20	DQ3R			
5B	VREFB5BN0	IO	CLK6n		DIFFIO_RX_R17n	DIFFOUT_R17n	K17				
5B	VREFB5BN0	IO			DIFFIO_TX_R18n	DIFFOUT_R18n	F20	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	H20	DQ3R			
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R20p	DIFFOUT_R20p	G18	DQ3R			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
5B	VREFB5BN0	IO			DIFFIO_RX_R19n	DIFFOUT_R19n	H19	DQ3R			
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R20n	DIFFOUT_R20n	G17	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_RX_R21p	DIFFOUT_R21p	K16	DQS3R			
5B	VREFB5BN0	IO			DIFFIO_TX_R22p	DIFFOUT_R22p	F19				
5B	VREFB5BN0	IO			DIFFIO_RX_R21n	DIFFOUT_R21n	J16	DQSn3R			
5B	VREFB5BN0	IO			DIFFIO_TX_R22n	DIFFOUT_R22n	F18	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_RX_R23p	DIFFOUT_R23p	J17	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_TX_R24p	DIFFOUT_R24p	J19	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	J18	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_TX_R24n	DIFFOUT_R24n	H18				
7A		GND					F17				
7A	VREFB7AN0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	H16			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	C21	DQ1T	DQ1T	T_DM_2	T_DM_2
7A	VREFB7AN0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	G16			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T18n	DIFFOUT_T18n	C20	DQ1T	DQ1T	T_DQ_23	T_DQ_23
7A	VREFB7AN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	D18	DQ1T	DQ1T	T_DQ_21	T_DQ_21
7A	VREFB7AN0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	B20	DQ1T	DQ1T	T_DQ_22	T_DQ_22
7A	VREFB7AN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	E17	DQ1T	DQ1T	T_DQ_20	T_DQ_20
7A	VREFB7AN0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	B21	DQ1T	DQ1T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	G15	DQS1T	DQS1T	T_DQS_2	T_DQS_2
7A	VREFB7AN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	B22			T_RESET#	T_RESET#
7A	VREFB7AN0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	G14	DQSn1T	DQSn1T	T_DQS#_2	T_DQS#_2
7A	VREFB7AN0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	A22	DQ1T	DQ1T	T_DQ_19	T_DQ_19
7A	VREFB7AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	E16	DQ1T	DQ1T	T_DQ_17	T_DQ_17
7A	VREFB7AN0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	A20	DQ1T	DQ1T	T_DQ_18	T_DQ_18
7A	VREFB7AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	D17	DQ1T	DQ1T	T_DQ_16	T_DQ_16
7A	VREFB7AN0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	A19			GND	GND
7A	VREFB7AN0	IO	CLK11p		DIFFIO_RX_T25p	DIFFOUT_T25p	G13				
7A	VREFB7AN0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	C19	DQ2T	DQ1T	T_DM_1	T_DM_1
7A	VREFB7AN0	IO	CLK11n		DIFFIO_RX_T25n	DIFFOUT_T25n	F14				
7A	VREFB7AN0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	C18	DQ2T	DQ1T	T_DQ_15	T_DQ_15
7A	VREFB7AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	C16	DQ2T	DQ1T	T_DQ_13	T_DQ_13
7A	VREFB7AN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	B16	DQ2T	DQ1T	T_DQ_14	T_DQ_14
7A	VREFB7AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	C15	DQ2T	DQ1T	T_DQ_12	T_DQ_12
7A	VREFB7AN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	B15	DQ2T	DQ1T	T_CKE_0	T_CKE_0
7A	VREFB7AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	G12	DQS2T	DQ1T	T_DQS_1	T_DQS_1
7A	VREFB7AN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	A18			T_CKE_1	T_CKE_1
7A	VREFB7AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	H12	DQSn2T	DQ1T	T_DQS#_1	T_DQS#_1
7A	VREFB7AN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	A17	DQ2T	DQ1T	T_DQ_11	T_DQ_11
7A	VREFB7AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	F15	DQ2T	DQ1T	T_DQ_9	T_DQ_9
7A	VREFB7AN0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	B18	DQ2T	DQ1T	T_DQ_10	T_DQ_10
7A	VREFB7AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	E14	DQ2T	DQ1T	T_DQ_8	T_DQ_8
7A	VREFB7AN0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	B17			GND	GND
7A	VREFB7AN0	IO	CLK10p		DIFFIO_RX_T33p	DIFFOUT_T33p	H10				
7A	VREFB7AN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	A15	DQ3T		T_DM_0	T_DM_0
7A	VREFB7AN0	IO	CLK10n		DIFFIO_RX_T33n	DIFFOUT_T33n	G11				
7A	VREFB7AN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	A14	DQ3T		T_DQ_7	T_DQ_7
7A	VREFB7AN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	D13	DQ3T		T_DQ_5	T_DQ_5
7A	VREFB7AN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	C14	DQ3T		T_DQ_6	T_DQ_6
7A	VREFB7AN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	C13	DQ3T		T_DQ_4	T_DQ_4
7A	VREFB7AN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	D14	DQ3T		T_ODT_1	T_ODT_1
7A	VREFB7AN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	H9	DQS3T		T_DQS_0	T_DQS_0
7A	VREFB7AN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	A13			T_ODT_0	T_ODT_0
7A	VREFB7AN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	G8	DQSn3T		T_DQS#_0	T_DQS#_0
7A	VREFB7AN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	B13	DQ3T		T_DQ_3	T_DQ_3
7A	VREFB7AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	E12	DQ3T		T_DQ_1	T_DQ_1
7A	VREFB7AN0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	B12	DQ3T		T_DQ_2	T_DQ_2
7A	VREFB7AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	F12	DQ3T		T_DQ_0	T_DQ_0
7A	VREFB7AN0	IO	RZQ_2		DIFFIO_TX_T40n	DIFFOUT_T40n	A12				
8A	VREFB8AN0	IO	CLK9p		DIFFIO_RX_T41p	DIFFOUT_T41p	G10				
8A	VREFB8AN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	C11	DQ4T		T_A_0	T_CA_0
8A	VREFB8AN0	IO	CLK9n		DIFFIO_RX_T41n	DIFFOUT_T41n	F10				
8A	VREFB8AN0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	B11	DQ4T		T_A_1	T_CA_1
8A	VREFB8AN0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	D11	DQ4T		T_A_4	T_CA_4
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T44p	DIFFOUT_T44p	A8	DQ4T		T_A_2	T_CA_2
8A	VREFB8AN0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	E11	DQ4T		T_A_5	T_CA_5
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T44n	DIFFOUT_T44n	A7	DQ4T		T_A_3	T_CA_3
8A	VREFB8AN0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	J9	DQS4T		T_CK	T_CK
8A	VREFB8AN0	IO			DIFFIO_TX_T46p	DIFFOUT_T46p	F8			T_A_6	T_CA_6
8A	VREFB8AN0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	J8	DQSn4T		T_CK#	T_CK#
8A	VREFB8AN0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	E7	DQ4T		T_A_7	T_CA_7
8A	VREFB8AN0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	C10	DQ4T		T_BA_1	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
8A	VREFB8AN0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	C6	DQ4T		T_BA_0	
8A	VREFB8AN0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	C9	DQ4T		T_BA_2	
8A	VREFB8AN0	IO			DIFFIO_TX_T48n	DIFFOUT_T48n	D7			GND	GND
8A	VREFB8AN0	IO	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T49p	DIFFOUT_T49p	K7				
8A	VREFB8AN0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	A10	DQ5T		T_CAS#	
8A	VREFB8AN0	IO	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T49n	DIFFOUT_T49n	J7				
8A	VREFB8AN0	IO			DIFFIO_TX_T50n	DIFFOUT_T50n	A9	DQ5T		T_RAS#	
8A	VREFB8AN0	IO			DIFFIO_RX_T51p	DIFFOUT_T51p	D9	DQ5T		T_A_8	T_CA_8
8A	VREFB8AN0	IO			DIFFIO_TX_T52p	DIFFOUT_T52p	B6	DQ5T		T_A_10	
8A	VREFB8AN0	IO			DIFFIO_RX_T51n	DIFFOUT_T51n	D8	DQ5T		T_A_9	T_CA_9
8A	VREFB8AN0	IO			DIFFIO_TX_T52n	DIFFOUT_T52n	B5	DQ5T		T_A_11	
8A	VREFB8AN0	IO			DIFFIO_RX_T53p	DIFFOUT_T53p	H8	DQS5T		T_CS#_0	T_CS#_0
8A	VREFB8AN0	IO			DIFFIO_TX_T54p	DIFFOUT_T54p	C8			T_A_12	
8A	VREFB8AN0	IO			DIFFIO_RX_T53n	DIFFOUT_T53n	G7	DQSn5T		T_CS#_1	T_CS#_1
8A	VREFB8AN0	IO			DIFFIO_TX_T54n	DIFFOUT_T54n	B8	DQ5T		T_A_13	
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	H6	DQ5T		T_A_14	
8A	VREFB8AN0	IO			DIFFIO_TX_T56p	DIFFOUT_T56p	E6	DQ5T		T_WE#	
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	G6	DQ5T		T_A_15	
8A	VREFB8AN0	IO			DIFFIO_TX_T56n	DIFFOUT_T56n	F7			GND	GND
9A		MSEL0		MSEL0			L6				
9A		CONF_DONE		CONF_DONE			J6				
9A		MSEL1		MSEL1			K6				
9A		nSTATUS		nSTATUS			G5				
9A		nCE		nCE			H5				
9A		MSEL2		MSEL2			A2				
9A		MSEL3		MSEL3			E5				
9A		nCONFIG		nCONFIG			A4				
9A		MSEL4		MSEL4			C5				
9A		GND					F3				
		GND					G4				
		GND					F5				
		GND					V4				
		GND					U4				
		GND					F21				
		GND					AB19				
		GND					AB2				
		GND					AB1				
		GND					AA16				
		GND					AA11				
		GND					AA4				
		GND					AA3				
		GND					Y13				
		GND					Y8				
		GND					Y5				
		GND					Y2				
		GND					Y1				
		GND					W20				
		GND					W4				
		GND					W3				
		GND					V22				
		GND					V17				
		GND					V2				
		GND					V1				
		GND					U19				
		GND					U14				
		GND					U9				
		GND					U5				
		GND					U3				
		GND					T11				
		GND					T2				
		GND					T1				
		GND					R13				
		GND					R3				
		GND					P10				
		GND					P4				
		GND					P2				
		GND					P1				
		GND					N22				
		GND					N15				
		GND					N13				
		GND					N11				
		GND					N7				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
		GND					N5				
		GND					N3				
		GND					M19				
		GND					M14				
		GND					M12				
		GND					M9				
		GND					M4				
		GND					M2				
		GND					M1				
		GND					L16				
		GND					L13				
		GND					L11				
		GND					L5				
		GND					L3				
		GND					K14				
		GND					K12				
		GND					K10				
		GND					K8				
		GND					K4				
		GND					K2				
		GND					K1				
		GND					J20				
		GND					J15				
		GND					J13				
		GND					J11				
		GND					J5				
		GND					J3				
		GND					H14				
		GND					H4				
		GND					H3				
		GND					H2				
		GND					H1				
		GND					G9				
		GND					G3				
		GND					F16				
		GND					F11				
		GND					F6				
		GND					F2				
		GND					F1				
		GND					E13				
		GND					E4				
		GND					E3				
		GND					D20				
		GND					D10				
		GND					D5				
		GND					D2				
		GND					D1				
		GND					C22				
		GND					C17				
		GND					C7				
		GND					C4				
		GND					C3				
		GND					B14				
		GND					B2				
		GND					B1				
		GND					A21				
		GND					A11				
		GND					A5				
		VCC					J14				
		VCC					P15				
		VCC					P13				
		VCC					P11				
		VCC					N14				
		VCC					N12				
		VCC					M15				
		VCC					M13				
		VCC					M11				
		VCC					L14				
		VCC					L12				
		VCC					L10				
		VCC					K13				
		VCC					K11				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
		VCC					K9				
		VCC					J12				
		VCC					J10				
		VCC					H15				
		VCC					H13				
		VCC					H11				
		VCC					P3				
		VCC					K3				
		VCC					L4				
		VCC					N4				
		VCC					K5				
		VCC					J4				
		DNU					B3				
		DNU					B4				
		DNU					D21				
		DNU					E10				
		VCCPGM					Y6				
		VCCPGM					U20				
		VCCPGM					B7				
		VCCBAT					A3				
		VCCIO3A					T6				
		VCCIO3A					AA6				
		VCCIO3B					V7				
		VCCIO3B					AB9				
		VCCIO3B					W10				
		VCCIO3B					R8				
		VCCIO4A					T16				
		VCCIO4A					AB14				
		VCCIO4A					AA21				
		VCCIO4A					Y18				
		VCCIO4A					W15				
		VCCIO4A					V12				
		VCCIO5A					T21				
		VCCIO5A					R18				
		VCCIO5B					H22				
		VCCIO5B					P20				
		VCCIO5B					N17				
		VCCIO5B					L21				
		VCCIO5B					K18				
		VCCIO5B					G19				
		VCCIO7A					B19				
		VCCIO7A					H17				
		VCCIO7A					E18				
		VCCIO7A					D15				
		VCCIO7A					C12				
		VCCIO7A					A16				
		VCCIO8A					E8				
		VCCIO8A					H7				
		VCCIO8A					B9				
		VCCIO8A					A6				
		VCCPD3A					V6				
		VCCPD3B4A					V16				
		VCCPD3B4A					W9				
		VCCPD3B4A					V14				
		VCCPD3B4A					V10				
		VCCPD5A					P17				
		VCCPD5B					N19				
		VCCPD5B					M18				
		VCCPD7A8A					F13				
		VCCPD7A8A					F9				
		VCCPD7A8A					E15				
		VCCPD7A8A					E9				
3A	VREFB3AN0	VREFB3AN0					W6				
3B	VREFB3BN0	VREFB3BN0					AB12				
4A	VREFB4AN0	VREFB4AN0					AA14				
5A	VREFB5AN0	VREFB5AN0					V21				
5B	VREFB5BN0	VREFB5BN0					K20				
7A	VREFB7AN0	VREFB7AN0					D16				
8A	VREFB8AN0	VREFB8AN0					B10				
		NC					AB3				
		NC					V11				
		NC					P22				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
		NC					P21				
		NC					P18				
		NC					P16				
		NC					N21				
		NC					N20				
		NC					N18				
		NC					N16				
		NC					M22				
		NC					M21				
		NC					M20				
		NC					L22				
		NC					K22				
		NC					J22				
		NC					F22				
		NC					E22				
		NC					C2				
		NC					C1				
		NC					G2				
		NC					G1				
		NC					L2				
		NC					L1				
		NC					R2				
		NC					R1				
		NC					W2				
		NC					W1				
		NC					AA2				
		NC					AA1				
		NC					D3				
		NC					D4				
		NC					E1				
		NC					E2				
		NC					J1				
		NC					J2				
		NC					N1				
		NC					N2				
		NC					U1				
		NC					U2				
		NC					Y3				
		NC					Y4				
		RREF_TL					A1				
		VCCA_FPLL					T4				
		VCCA_FPLL					F4				
		VCCA_FPLL					U18				
		VCCA_FPLL					E19				
		VCCA_FPLL					T3				
		VCCA_FPLL					M3				
		VCC_AUX					D6				
		VCC_AUX					D12				
		VCC_AUX					D19				
		VCC_AUX					W19				
		VCC_AUX					AA12				
		VCC_AUX					AB5				

Notes:
(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.
(2) RESET pin is only applicable for DDR3 device.

Version Number	Date	Changes Made
1.0	11/29/2012	Initial release.
1.1	7/4/2013	- Added M383 package. - Updated the column from "HMC Pin Assignment for DDR3" to "HMC Pin Assignment for DDR3/DDR2". - Added note to the "HMC Pin Assignment for DDR3/DDR2" column.