How to constrain PLL outputs when using clock switchover in Stratix® V, Arria® V, or Cyclone® V devices

Description:

In the Quartus® II software, the `derive_pll_clocks` Synopsys Design Constraint (SDC) command creates generated clock constraints for PLL outputs. PLL clock switchover allows a PLL to have multiple reference clock inputs. In general, the `derive_pll_clocks` command supports designs with PLL clock switchover and constrains the PLL outputs relative to each reference clock input. However, for devices using the Altera_PLL megafunction, including Stratix V, Arria V and Cyclone V devices, the `derive_pll_clocks` command creates the generated clocks on PLL outputs relative to the first input clock only. To constrain the PLL outputs relative to the remaining input clocks, replace the `derive_pll_clocks` command with `create_generated_clock` SDC commands to constrain the VCO and output counter clocks relative to each input clock.

This document describes how to create the `create_generated_clock` commands to constrain your PLL outputs relative to multiple reference clock inputs. Following this description are example constraints of how to apply these instructions. The example constraints refer to an example design contained in the Quartus II archive **top_clock_swtichover_example_design.qar**. This archive is available for download from http://www.altera.com/support/kdb/solutions/rd10162012_514.html.

Steps to create clock switchover constraints:

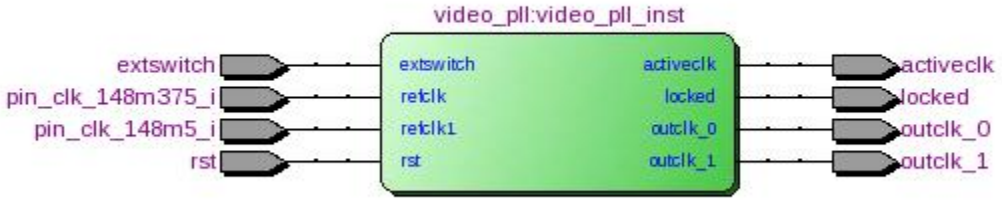
1. Compile your design in the Quartus II software.
2. Open the TimeQuest timing analyzer GUI and create the timing netlist.
3. At the Tcl prompt in the Console pane, run `derive_pll_clocks`. The TimeQuest timing analyzer console displays a set of `create_generated_clock` commands constraining your PLL relative to the first reference clock input. There will be multiple `create_generated_clock` commands for the VCO clocks internal to the PLL. These generated clock names end in `fpll|vcoph[n]`. There will also be one `create_generated_clock` command for each output counter corresponding to each PLL output clock. These generated clock names end in `counter[n].output_counter|divclk`. See the constraints for the example design in Table 1 below.
4. Copy these `create_generated_clock` commands to your Synopsys Design Constraints (**.sdc**) file and modify the constraints for the first reference clock as follows:

a) For the `create_generated_clock` constraint for each VCO clock, change the source to the pin name for the first reference clock and add the `-master_clock` option and specify the clock created on the reference clock input.
b) Because PLL node names may change with each compilation, modify the `create_generated_clock` constraint for each output counter clock to use wildcards. For example, change source names that end with `vco1ph[0]` to end with `vco*ph[*]`.
    - See the following solution for further details on this change: http://www.altera.com/support/kdb/solutions/rd10042012_164.html
c) For each output counter `create_generated_clock` constraints, add the option `-master_clock` and specify the master clock. Run the Report Clocks task in the TimeQuest timing analyzer to verify the master clock for each output counter clock.

5. Create similar sets of constraints for both VCO and output counter clocks relative to each remaining reference clock. Note that clock names need to be unique, so change the names for the VCO and output counter clocks.
6. Because only one set of clocks is active at any given time, paths between different sets of clocks can be cut using the `set_clock_groups` command.

Design example description:

The attached design **top_clock_swtichover_example_design.qar** has the following top-level representation



The above PLL has two reference clocks **pin_clk_148m375_i** and **pin_clk_148m5_i** and the PLL switches between these two clocks.

Table 1 shows the constraints created by default for this design using the `derive_pll_clocks` command.

```
create_generated_clock -source
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|counter[0].output_co
unter|vco1ph[0]} -divide_by 4 -duty_cycle 50.00 -name
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|counter[0].output_co
unter|divclk}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|counter[0].output_co
unter|divclk}

create_generated_clock -source
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|counter[1].output_co
unter|vco1ph[0]} -divide_by 2 -duty_cycle 50.00 -name
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|counter[1].output_co
unter|divclk}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|counter[1].output_co
unter|divclk}

create_generated_clock -source
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|refclkin
} -multiply_by 4 -duty_cycle 50.00 -name
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[0]
}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[0]
}

create_generated_clock -source
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|refclkin
} -multiply_by 4 -duty_cycle 50.00 -name
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[1]
}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[1]
}

create_generated_clock -source
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|refclkin
} -multiply_by 4 -duty_cycle 50.00 -name
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[2]
}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[2]
}

create_generated_clock -source
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|refclkin
} -multiply_by 4 -duty_cycle 50.00 -name
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[3]
}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[3]
}

create_generated_clock -source
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|refclkin
} -multiply_by 4 -duty_cycle 50.00 -name
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[4]
}
```

```
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[4]
}

create_generated_clock -source
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|refclkin
} -multiply_by 4 -duty_cycle 50.00 -name
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[5]
}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[5]
}

create_generated_clock -source
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|refclkin
} -multiply_by 4 -duty_cycle 50.00 -name
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[6]
}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[6]
}

create_generated_clock -source
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|refclkin
} -multiply_by 4 -duty_cycle 50.00 -name
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[7]
}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[7]
}
```

Table 1

Table 2 shows the modified constraints for the first reference clock.

```
create_generated_clock -source [get_ports pin_clk_148m375_i] -multiply_by 4 -
duty_cycle 50.00 -master_clock FPGA_CORE_CLK148M3 -name
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[0]
}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[0]
}

create_generated_clock -source [get_ports pin_clk_148m375_i] -multiply_by 4 -
duty_cycle 50.00 -master_clock FPGA_CORE_CLK148M3 -name
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[1]
}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[1]
}

create_generated_clock -source [get_ports pin_clk_148m375_i] -multiply_by 4 -
duty_cycle 50.00 -master_clock FPGA_CORE_CLK148M3 -name
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[2]
}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[2]
}

create_generated_clock -source [get_ports pin_clk_148m375_i] -multiply_by 4 -
duty_cycle 50.00 -master_clock FPGA_CORE_CLK148M3 -name
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[3]
}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[3]
}

create_generated_clock -source [get_ports pin_clk_148m375_i] -multiply_by 4 -
duty_cycle 50.00 -master_clock FPGA_CORE_CLK148M3 -name
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[4]
}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[4]
}

create_generated_clock -source [get_ports pin_clk_148m375_i] -multiply_by 4 -
duty_cycle 50.00 -master_clock FPGA_CORE_CLK148M3 -name
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[5]
}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[5]
}

create_generated_clock -source [get_ports pin_clk_148m375_i] -multiply_by 4 -
duty_cycle 50.00 -master_clock FPGA_CORE_CLK148M3 -name
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[6]
}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[6]
}

create_generated_clock -source [get_ports pin_clk_148m375_i] -multiply_by 4 -
duty_cycle 50.00 -master_clock FPGA_CORE_CLK148M3 -name
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[7]
}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[7]
```

```
}

create_generated_clock -source
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|counter[0].output_co
unter|vco*ph[*]} -divide_by 4 -duty_cycle 50.00 -master_clock
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[0]
} -name
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|counter[0].output_co
unter|divclk}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|counter[0].output_co
unter|divclk}

create_generated_clock -source
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|counter[1].output_co
unter|vco*ph[*]} -divide_by 2 -duty_cycle 50.00 -master_clock
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[0]
} -name
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|counter[1].output_co
unter|divclk}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|counter[1].output_co
unter|divclk}
```

Table 2

Table 3 shows the modified constraints for the second reference clock.

```
create_generated_clock -source [get_ports pin_clk_148m5_i] -multiply_by 4 -
duty_cycle 50.00 -master_clock FPGA_CORE_CLK148M5 -name
{two_video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcop
h[0]}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[0]
} -add

create_generated_clock -source [get_ports pin_clk_148m5_i] -multiply_by 4 -
duty_cycle 50.00 -master_clock FPGA_CORE_CLK148M5 -name
{two_video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcop
h[1]}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[1]
} -add

create_generated_clock -source [get_ports pin_clk_148m5_i] -multiply_by 4 -
duty_cycle 50.00 -master_clock FPGA_CORE_CLK148M5 -name
{two_video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcop
h[2]}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[2]
} -add

create_generated_clock -source [get_ports pin_clk_148m5_i] -multiply_by 4 -
duty_cycle 50.00 -master_clock FPGA_CORE_CLK148M5 -name
{two_video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcop
h[3]}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[3]
} -add

create_generated_clock -source [get_ports pin_clk_148m5_i] -multiply_by 4 -
duty_cycle 50.00 -master_clock FPGA_CORE_CLK148M5 -name
{two_video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcop
h[4]}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[4]
} -add

create_generated_clock -source [get_ports pin_clk_148m5_i] -multiply_by 4 -
duty_cycle 50.00 -master_clock FPGA_CORE_CLK148M5 -name
{two_video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcop
h[5]}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[5]
} -add

create_generated_clock -source [get_ports pin_clk_148m5_i] -multiply_by 4 -
duty_cycle 50.00 -master_clock FPGA_CORE_CLK148M5 -name
{two_video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcop
h[6]}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[6]
} -add

create_generated_clock -source [get_ports pin_clk_148m5_i] -multiply_by 4 -
duty_cycle 50.00 -master_clock FPGA_CORE_CLK148M5 -name
{two_video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcop
h[7]}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[7]
```

```
} -add

create_generated_clock -source
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|counter[0].output_co
unter|vco*ph[*]} -divide_by 4 -duty_cycle 50.00 -master_clock
{two_video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcop
h[0]} -name
{two_video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|counter[0].outpu
t_counter|divclk}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|counter[0].output_co
unter|divclk} -add

create_generated_clock -source
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|counter[1].output_co
unter|vco*ph[*]} -divide_by 2 -duty_cycle 50.00 -master_clock
{two_video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcop
h[0]} -name
{two_video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|counter[1].outpu
t_counter|divclk}
{video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|counter[1].output_co
unter|divclk} -add
```

Table 3

Table 4 shows how to cut paths between the two sets of clocks.

```
set_clock_groups -exclusive -group [get_clocks {FPGA_CORE_CLK148M3
video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[0]
video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[1]
video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[2]
video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[3]
video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[4]
video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[5]
video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[6]
video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph[7]
video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|counter[0].output_cou
nter|divclk
video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|counter[1].output_cou
nter|divclk}] -group [get_clocks {FPGA_CORE_CLK148M5
two_video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph
[0]
two_video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph
[1]
two_video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph
[2]
two_video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph
[3]
two_video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph
[4]
two_video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph
[5]
two_video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph
[6]
two_video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|fpll_0|fpll|vcoph
[7]
video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|counter[0].output_cou
nter|divclk
video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|counter[1].output_cou
nter|divclk}]
```

Table 4

Tip:

To shorten the name of the counter clocks so that you can use them in other constraints like `set_input_delay` or `set_ouput_delay`, you can create a Tcl variable to refer to the longer name. For example:

```
set CLK_C0
clocks_inst|video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|co
unter[0].output_counter|divclk

set CLK_C1
clocks_inst|video_pll_inst|video_pll_inst|altera_pll_i|stratixv_pll|co
unter[1].output_counter|divclk
```

```
set_output_delay –clock $CLK_CO …
```

Revision	Changes Made	Date
V1.0	Initial release.	November 2012