WHITE PAPER
Intel® Xeon® processor 3500 and 5500 series
Intel® Microarchitecture

First the Tick, Now the Tock: Intel® Microarchitecture (Nehalem)

"By measuring the benefit of the performance gain against the power cost, Intel was able to design Intel microarchitecture (Nehalem) to deliver greater power efficiency at any power envelope."

Jeff Casazza
Intel Corporation

Introducing a New Dynamically and Design-Scalable Microarchitecture that Rewrites the Book on Energy Efficiency and Performance

Since the introduction of Intel® Core™ microarchitecture in 2006 and its 2007 45nm enhancements—the Intel Core microarchitecture (Penryn) family of processors—the blistering performance and energy efficiency of Intel® microprocessors have delivered unprecedented capabilities to computer users. Now a new microarchitecture named Nehalem (the foundation of the Intel® Xeon® processor 3500 and 5500 series) builds on these earlier microarchitectural marvels, rewriting the book on processor scalability, performance, and energy efficiency.

The first chapter is all about scalability. Intel® microarchitecture (Nehalem) is a dynamically scalable and design-scalable microarchitecture. At runtime, it dynamically manages cores, threads, cache, interfaces, and power to deliver outstanding energy efficiency and performance on demand. At design time, it scales easily, enabling Intel to provide versions optimized for each server, desktop, and notebook market. Intel will deliver versions differing in the number of cores, caches, interconnect capability, and memory controller capability, as well as in the inclusion of an integrated graphics controller. This allows Intel to deliver a wide range of price, performance, and energy efficiency targets for servers, workstations, desktops, and laptops.

Intel microarchitecture's (Nehalem's) energy efficiency and performance comes at a critical crossroads in computing. In the past, when a computer's energy efficiency wasn't a concern, nearly every architecture feature that could improve processor performance would be included without worrying about the power cost. But in an age of increasing concern for limited resources and increased energy costs, every segment (server, workstation, desktop, and mobile) is power-constrained and designing a microarchitecture requires a different approach. Processor manufacturers must consider the power cost for whether the processor is intended for the home, data center, or ultra-light laptop.

Intel weighed every architectural feature added to Intel microarchitecture (Nehalem) against a strict power/performance efficiency threshold. If the feature couldn't add more than a one percent performance gain for a less than three percent power cost, Intel wouldn't add it. By measuring the benefit of the performance gain against the power cost, Intel was able to design Intel microarchitecture (Nehalem) to deliver greater power efficiency at any power envelope.

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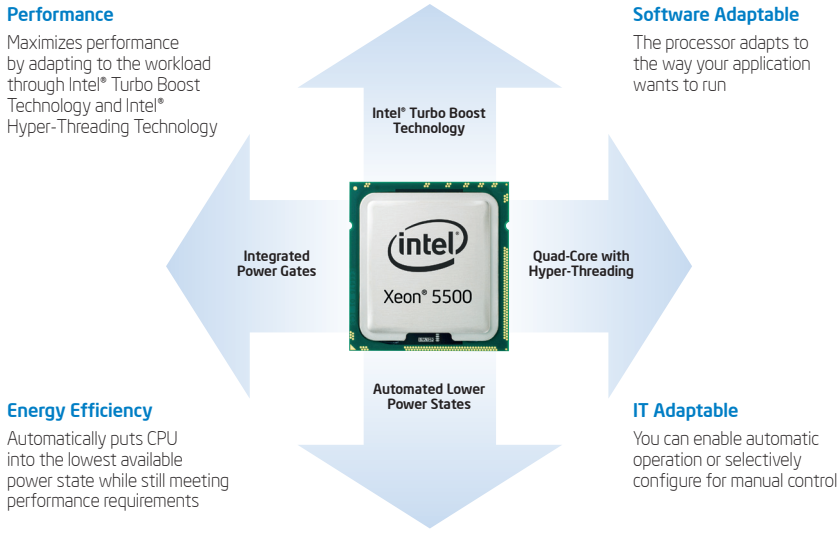
The Adaptability of the Intel® Xeon® Processor 3500 and 5500 Series



Example: Intel® Xeon® Processor 3500 and 5500 Series

A good example of how Intel microarchitecture (Nehalem) enables the scaling of energy efficiency and performance can be seen in the Intel Xeon processor 3500 and 5500 series. These two server/workstation processor series incorporate a number of Intel's innovative technologies to deliver intelligent performance. (Each of which will be discussed in more depth later in this paper.)

- **Intel® Turbo Boost Technology.** This technology (in combination with Intel® Intelligent Power Technology described below), delivers performance on demand, allowing processors to operate above the rated frequency to speed specific workloads and drop back down to reduce power consumption during low utilization periods.
- **Intel® Hyper-Threading Technology.**[1] This well-known Intel innovation provides more performance for applications designed for parallel, multi-threaded execution by reducing computational latency and making optimal use of every cycle. Intel® Hyper-Threading Technology benefits from this latest Intel microarchitecture's larger caches and massive memory bandwidth, delivering greater throughput and responsiveness for multi-threaded applications.
- **Intel® QuickPath Technology.** This new, scalable, shared memory architecture integrates a memory controller into each microprocessor and connects processors and other components with a new high-speed interconnect. It speeds traffic between processors and I/O controllers for bandwidth-intensive applications, delivering up to 3.5 times the bandwidth for technical computing.[2]
- **Intel® Intelligent Power Technology.** This feature enables policy-based control that allows processors to operate at optimal frequency and power. Operating systems can make this determination automatically, or administrators can designate which applications require high-frequency processing and which should be executed at lower frequencies to conserve power.[3]
- **Intel® Virtualization Technology.**[4] This latest generation version of Intel® Virtualization Technology (Intel® VT) enhances virtualization performance by up to 2.1 times[5] with new hardware-assist capabilities across server and workstation elements.

Unlocking All the Power of Intel's 45nm Hi-k Metal Gate Process Technology

Intel microarchitecture (Nehalem) marks the next step (a "tock") in Intel's rapid "tick-tock" cadence for delivering a new process technology (tick) or an entirely new microarchitecture (tock) every year.

Intel microarchitecture (Nehalem) was designed from the ground up to capitalize on all the advantages of Intel's industry-leading 45-nanometer (nm) Hi-k metal gate silicon technology. This process technology is one of the biggest advancements in fundamental transistor design in 40 years. It uses a unique material combination of Hi-k gate dielectrics and conductors to enable Intel to continue record-breaking PC, laptop, and server processor performance while reducing the electrical leakage from transistors that can hamper chip and PC design, size, power consumption, and costs.

Intel's 45nm Hi-k silicon process technology increases transistor switching speeds to enable higher core and bus clock frequencies and thus more performance in the same power and thermal envelope. This performance efficiency is helping Intel extend Moore's Law (a high-tech industry axiom that transistor counts double about every two years to deliver ever more functionality at exponentially decreasing cost) well into the next decade.

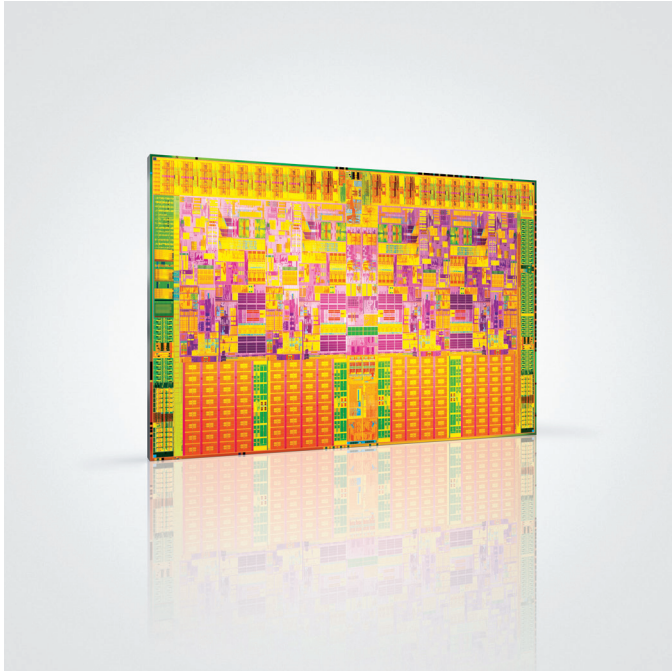


Figure 1. Intel® microarchitecture (Nehalem).

An Overview of Intel's New Microarchitecture

Intel microarchitecture (Nehalem) continues Intel's philosophy of focusing on improvements in how the processor uses available clock cycles and power, rather than just pushing up ever higher clock speeds and energy needs. The goal is to do more in the same power envelope—or even reduced envelopes. In turn, like its Intel Core microarchitecture predecessor (Penryn), Intel microarchitecture (Nehalem) includes the ability to process up to four instructions per clock cycle on a sustained basis compared to just three instructions per clock cycle or less processed by other processors. However, the biggest innovations offered by Intel microarchitecture (Nehalem) come from new optimizations of the individual cores and the overall multi-core microarchitecture to increase single-thread and multi-thread performance.

Intel microarchitecture (Nehalem) includes these performance and power management innovations:

- Dynamically managed cores, threads, cache, interfaces, and power
- Intel Hyper-Threading Technology, a capability which enables running two simultaneous threads per core—an amazing eight simultaneous threads per quad-core processor and 16 simultaneous threads for dual-processor, quad-core designs. This feature provides an energy efficient means of increasing performance for multi-threaded workloads.
- Innovative extensions to the Intel® Streaming SIMD Extensions 4 (SSE4) that center on enhancing Extensible Markup Language (XML), string, and text processing performance
- Superior multi-level cache, including an inclusive shared L3 (last-level) cache
- New high-end system architecture that delivers from two to three times more peak bandwidth and up to four times more realized bandwidth (depending on configuration) as compared to previous Intel Xeon processors
- Performance-enhanced dynamic power management

On the design side, Intel microarchitecture (Nehalem) enables optimal price/performance/energy efficiency for each market segment through:

- Scalable performance for from one-to-16 (or more) threads and from one-to-eight (or more) cores
- Scalable and configurable system interconnects and integrated memory controllers
- High-performance integrated graphics engine for client platforms

An In-Depth Look at Top Features

We will now provide a more in-depth look at some of the top features of Intel microarchitecture (Nehalem) that are available in the Intel Xeon processor 3500 and 5500 series.

1. Intel® Turbo Boost Technology

Intel® Turbo Boost Technology is an innovative feature that automatically allows active processor cores to run faster than the base operating frequency when there is available headroom within power, current, and temperature specification limits. This enables Intel Xeon processor 3500 and 5500 series to deliver extra performance when and where it is needed (see Figure 2). This can be particularly advantageous in speeding up the processing of light or lightly threaded workloads.

Higher Performance on Demand

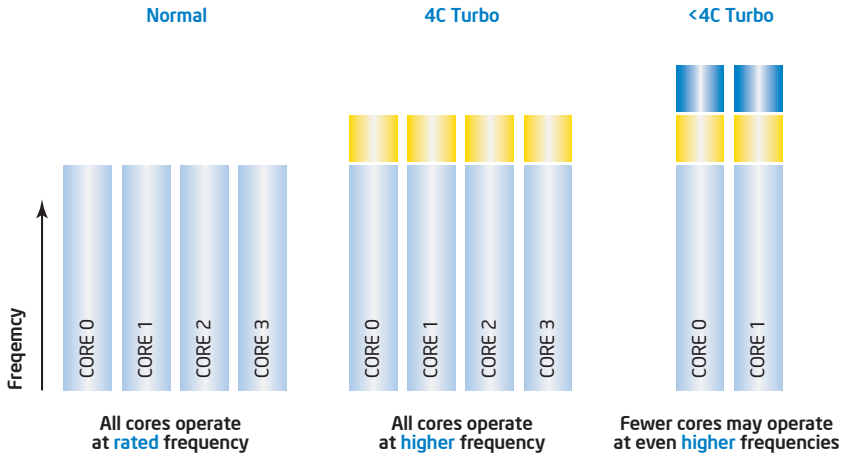


Figure 2. Intel® Turbo Boost Technology increases performance by increasing processor frequency and enabling faster speeds when conditions allow.

Intel Turbo Boost Technology is activated when the operating system requests the highest processor performance state. Headroom is dynamically assessed by continual measurement of temperature, current draw, and power consumption. The maximum frequency of Intel Turbo Boost Technology is dependent on the number of active cores. The amount of time the processor spends in the Intel Turbo Boost Technology state depends on the workload and operating environment.

Any of the following can set the upper limit of Intel Turbo Boost Technology on a given workload:

- Number of active cores
- Estimated current consumption
- Estimated power consumption
- Processor temperature

The number of active cores at any given instant dictates the upper limit of Intel Turbo Boost Technology. For instance, a core is considered "active" if it is in the "C0" or "C1" state; a core in the "C3" or "C6" state is considered "inactive." (C-states are the power conservation states of a processor core.) The upper limits will vary on a per-processor number basis. For example, a particular processor may allow up to two frequency steps (266.66 MHz) when just one core is active and one frequency step (133.33 MHz) when two or more cores are active. Therefore, higher C-state residency ("C3" or "C6") on some cores will generally result in increased core frequency on the active cores.

The upper limits are further constrained by temperature, power, and current. These constraints are managed as a simple closed-loop control system. If measured temperature, power, and current are all below factory-configured limits, and the operating system (OS) is requesting maximum processor performance, the processor automatically steps up core frequency (+133.33 MHz) until it reaches the upper limit dictated by the number of active cores. When temperature, power, or current exceed factory-configured limits—and you are above the base operating frequency—the processor automatically steps down core frequency (-133.33 MHz) in order to reduce temperature, power, and current. The processor then monitors temperature, power, and current, and continuously re-evaluates.

Note: When Intel Turbo Boost Technology is requested by the OS, the processor will commonly operate between the maximum Intel Turbo Boost Technology frequency and the base operating frequency. All active cores in the processor will operate at the same frequency. Even at frequencies above the base operating frequency, all active cores will run at the same frequency and voltage. Due to the way the system firmware and OS communicate, the software may never detect core clock frequencies above the operating frequency.[5]

2. Intel® Hyper-Threading Technology

Many server and workstation applications lend themselves to parallel, multi-threaded execution. Intel Hyper-Threading Technology enables simultaneous multi-threading within each processor core, up to two threads per core or eight threads per quad-core processor (see Figure 3, next page). Hyper-threading reduces computational latency, making optimal use of every clock cycle. For example, while one thread is waiting for a result or event, another thread is executing in that core to maximize the work from each clock cycle.

An Intel® processor and chipset combined with an operating system and system firmware supporting Intel Hyper-Threading Technology enables:

- Running demanding applications simultaneously while maintaining system responsiveness
- Running multi-threaded applications faster to maximize productivity and performance
- Increasing the number of transactions that can be processed simultaneously
- Providing headroom for new solution capabilities and future needs

When Intel Hyper-Threading Technology and Intel Turbo Boost Technology are combined in processors based on Intel microarchitecture (Nehalem), these intelligent processors deliver better performance by dynamically adapting to the workload. They automatically take advantage of available headroom to increase processor frequency and maximize clock cycles on active cores to get the tasks done quicker.

3. Other Key Performance Improvement Features

Intel microarchitecture (Nehalem) includes significant core enhancements to further improve the performance of the individual processor cores. Below we describe some of these enhancements.

Intel® Smart Cache Enhancements

Intel microarchitecture (Nehalem) enhances the Intel® Smart Cache by adding an inclusive shared L3 cache that can be up to eight megabytes (MB) in size. In addition to this cache being shared across all cores, the inclusive shared L3 cache can increase performance while reducing traffic to the processor cores. Some architectures use exclusive L3 cache, which contains data not stored in other caches. Thus, if a data request misses on the L3 cache, each processor core must still be searched (or snooped) in case their individual caches might contain the requested data. This can increase latency and snoop traffic between cores. With Intel microarchitecture (Nehalem), a miss of its inclusive shared L3 cache guarantees the data is outside the processor and thus is designed to eliminate unnecessary core snoops to reduce latency and improve performance.

The new three-level cache hierarchy for Intel microarchitecture (Nehalem) consists of:

- Same L1 cache as Intel Core microarchitecture (32 KB Instruction Cache, 32 KB Data Cache)
- New L2 cache per core for very low latency (256 KB per core for handling data and instruction)
- New fully inclusive, fully shared 8 MB L3 cache (all applications can use entire cache)

Intel® Hyper-Threading Technology

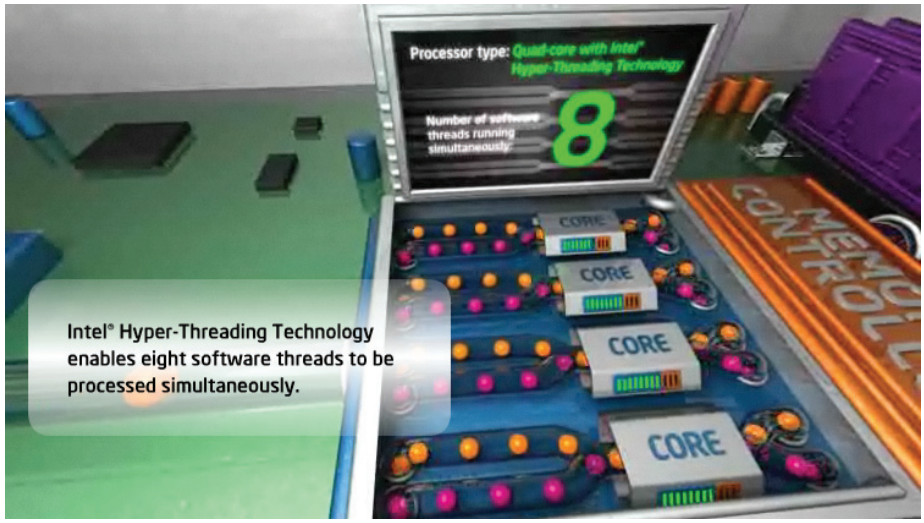


Figure 3. Intel® Hyper-Threading Technology enables simultaneous multi-threading of eight threads per quad-core processor.

A new two-level Translation Lookaside Buffer (TLB) hierarchy is also included in Intel microarchitecture (Nehalem). A TLB is a processor cache that is used by memory management hardware to improve the speed of virtual address translation. The TLB references physical memory addresses in its table. All current desktop and server processors use a TLB, but Intel microarchitecture (Nehalem) adds a new second level 512 entry TLB to further improve performance.

Instructions per Cycle Improvements

The more instructions that can be run each clock cycle, the greater the performance. In many cases, by running more instructions in any given clock cycle, the work task can complete sooner, enabling the processor to more quickly return to a lower power state. To run more instructions per cycle, Intel made several key innovations.

- Greater Parallelism. One way to extract more parallelism out of software code is to increase the amount of instructions that can be run "out of order." This enables more simultaneous processing. To be able to identify more independent operations that can be run in parallel, Intel increased the size of the out-of-order window and scheduler, giving them a wider window from which to look for these operations. Intel also increased the size of the other buffers in the core to ensure they wouldn't become a limiting factor.
- More Efficient Algorithms. With each new microarchitecture, Intel has included improved algorithms in places where previous processor generations saw lost performance due to stalls (dead cycles). Intel microarchitecture (Nehalem) brings many such improved algorithms to increase performance. These include:
  - Faster Synchronization Primitives: As multi-threaded software becomes more prevalent, the need to synchronize threads is also becoming more common. Intel microarchitecture (Nehalem) speeds up the common legacy synchronization primitives (such as instructions with a LOCK prefix or the XCHG instruction) so that existing threaded software will see a performance boost.
  - Faster Handling of Branch Mispredictions: A common way to increase performance is through the prediction of branches. Intel microarchitecture (Nehalem) optimizes the cases where the predictions are wrong, so that the effective penalty of branch mispredictions overall is lower than on prior processors.

– Improved Hardware Prefetch and Better Load-Store Scheduling: Intel microarchitecture (Nehalem) continues the many advances Intel made with the Intel Core microarchitecture (Penryn) family of processors in reducing memory access latencies through prefetch and load-store scheduling improvements.

Enhanced Branch Prediction

Branch prediction attempts to guess whether a conditional branch will be taken or not. Branch predictors are crucial in today's processors for achieving high performance. They allow processors to fetch and execute instructions without waiting for a branch to be resolved. Processors also use branch target prediction to attempt to guess the target of the branch or unconditional jump before it is computed by parsing the instruction itself. In addition to greater performance, an additional benefit of increased branch prediction accuracy is that it can enable the processor to consume less energy by spending less time executing mispredicted branch paths.

Intel microarchitecture (Nehalem) uses several innovations to reduce branch mispredicts that can hinder performance and to improve the handling of branch mispredicts.

- New Second-Level Branch Target Buffer (BTB). To improve branch predictions in applications that have large code footprints (e.g., database applications), Intel added a second-level branch target buffer. BTBs reduce the performance penalty of branches in pipelined processors by predicting the path of the branch and caching information used by the branch.
- New Renamed Return Stack Buffer (RSB). RSBs store forward and return pointers associated with call and return instructions. Intel's new renamed RSB helps avoid many common return instruction mispredictions.

New Application Targeted Accelerators and Intel® SSE4

Intel microarchitecture (Nehalem) includes all the additional Intel SSE4 instructions Intel included in Intel Core microarchitecture (Penryn) for faster computation/manipulation of media (graphics, video encoding and processing, 3-D imaging, and gaming). In addition, Intel microarchitecture (Nehalem) adds seven new Application Targeted Accelerators for more efficient accelerated string and text processing of applications like XML.

Application Targeted Accelerators extend the capabilities of Intel® architecture by adding performance-optimized, low-latency, lower power fixed-function accelerators on the processor die to benefit specific applications. Such accelerators are the start of a natural evolution where gradually more and more advantageous implementations of fixed-function capabilities will be developed and added to the processor. Just as the evolution of silicon technology from 65nm to 45nm to 32nm enables more transistors for additional cores and cache, so too will it also enable more of these fixed-function on-die implementations. The benefit will be greater performance—and superior energy efficiency—for these specific applications.

The seven Application Targeted Accelerators included in Intel microarchitecture (Nehalem) provide new string and text processing instructions to improve performance of string and text processing operations. For example, they enable parsing of XML strings and text at a much higher speed. These Application Targeted Accelerators will be useful for lexing, tokenizing, regular expression evaluation, virus scanning, and intrusion.

Improved Virtualization Performance

Virtualization partitions a computer so that it can run separate operating systems and software in each partition, allowing one computer to act as many. Virtualization enables computers, particularly servers, to better leverage multi-core processing power and increase efficiency. Intel microarchitecture (Nehalem) adds new features that enable software to further improve their performance in virtualized environments. For example, Intel microarchitecture (Nehalem) includes an Extended Page Table (EPT) for reconciling memory type specification in a guest operating system with memory type specification in the host operating system in virtualization systems that support memory type specification.

4. New System Architecture: Intel® QuickPath Technology

To deliver top performance for bandwidth-intensive applications, the Intel Xeon processor 3500 and 5500 series feature Intel® QuickPath Technology (see Figure 4, next page). As mentioned earlier in this paper, this new scalable, shared memory architecture delivers memory bandwidth leadership at up to 3.5 times the bandwidth of previous-generation processors.

Intel QuickPath Technology is a platform architecture that provides high-speed (up to 25.6 GB/s), point-to-point connections between processors, and between processors and the I/O hub. Each processor has its own dedicated memory that it accesses directly through an Integrated Memory Controller. In cases where a processor needs to access the dedicated memory of another processor, it can do so through a high-speed Intel® QuickPath Interconnect that links all the processors.

Intel microarchitecture (Nehalem) complements the benefits of Intel QuickPath Interconnect by enhancing Intel Smart Cache with an inclusive shared L3 cache that boosts performance while reducing traffic to the processor cores.

Intel® QuickPath Interconnect Performance

Intel QuickPath Interconnect 's throughput clearly demonstrates its best-in-class interconnect performance in the server/workstation market segment.

- Intel QuickPath Interconnect uses up to 6.4 Gigatranfers/second links, delivering up to 25 Gigabytes/second (GB/s) of total bandwidth. That's up to 300 percent greater than any other interconnect solution used previously. (Gigatransfer refers to the number of data transfers or operations.)
- Intel QuickPath Interconnect 's superior architecture reduces the amount of communication required in the interface of multi-processor systems to deliver faster payloads.
- Intel QuickPath Interconnect Implicit Cyclic Redundancy Check (CRC) with link-level retry ensures data quality and performance by providing CRC without the performance penalty of additional cycles.

Intel® QuickPath Technology

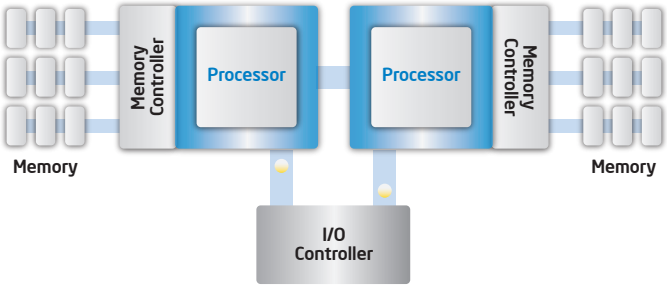


Figure 4. Intel® QuickPath Technology provides dedicated per-processor memory and point-to-point connectivity.

5. Intel® Intelligent Power Technology

Intel Intelligent Power Technology is an innovation that monitors power consumption in servers to identify those that are not being fully utilized. It has two main features:

- Integrated Power Gates (see Figure 5) allow individual idling cores to be reduced to near-zero power independent of other operating cores, reducing idle power consumption to 10 watts, versus 16 or 50 watts in prior generations of Intel quad-core processors.[7]
- Automated Low-Power States automatically put processor and memory into the lowest available power states that will meet the requirement of the current workload (see Figure 6). Because processors are enhanced with more and lower CPU power states, and the memory and I/O controllers have new power management features, the degree to which power can be minimized is now greatly enhanced.

6. Intel® Virtualization Technology

Next-generation Intel Virtualization Technology (Intel VT) enhances virtualization performance with new hardware-assist capabilities across all elements of your server and workstation.

Processor: Improvements to Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x) provide hardware-assisted page-table management, allowing the guest OS more direct access to the hardware and reducing compute-intensive software translation from the virtual machine monitor (VMM). Intel VT-x also includes Intel® Virtualization Technology FlexMigration and Intel® Virtualization Technology FlexPriority, which are capabilities for flexible workload migration and performance optimization across the full range of 32-bit and 64-bit operating environments.

Automatic Operation or Manual Core Control

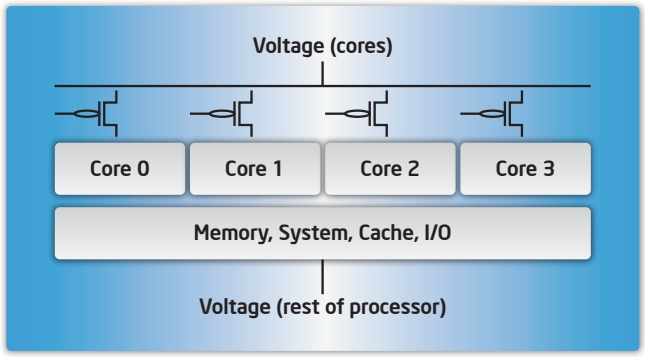


Figure 5. Integrated Power Gates enable idle cores to go to near-zero power independently.

Chipset: Intel® Virtualization Technology for Directed I/O (Intel® VT-d) helps speed data movement and eliminates much of the performance overhead by giving designated virtual machines their own dedicated I/O devices, thus reducing the overhead of the VMM in managing I/O traffic.

Network Adapter: Intel® Virtualization for Connectivity (Intel® VT-c) further enhances server I/O solutions by integrating extensive hardware assists into the I/O devices that are used to connect servers to the data center network, storage infrastructure, and other external devices. By performing routing functions to and from virtual machines in dedicated network silicon, Intel VT-c speeds delivery and reduces the load on the VMM and server processors, providing up to two times the throughput of non-hardware-assisted devices.[8]

Automated Low-Power States

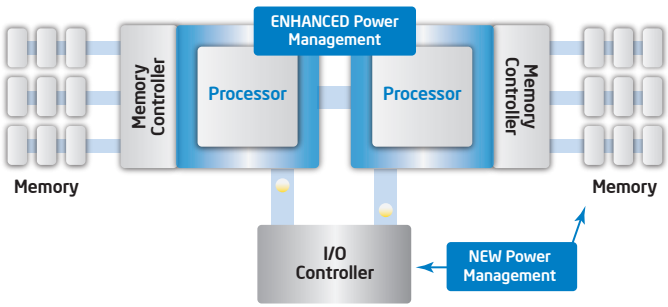


Figure 6. Automated Low-Power States adjust system power consumption based on real-time load.

Summary

Intel microarchitecture (Nehalem) represents the next level of multi-core performance, offering the latest in processor innovation. First appearing as the Intel® Core™ i7 processor and now the foundation for the Intel Xeon processor 3500 and 5500 series, Intel microarchitecture (Nehalem) intelligently maximizes performance to match workloads. As a microarchitecture for server/workstation processors, it offers energy-efficient performance that scales energy use per performance demands while unleashing parallel processing performance. Its new, scalable, shared memory architecture integrates a memory controller into each microprocessor and connects processors and other components with a new high-speed interconnect that speeds traffic between processors and I/O controllers for bandwidth-intensive applications. Numerous virtualization technologies enable Intel microarchitecture (Nehalem) to offer best-in-class virtualization, making it the obvious choice for consolidation projects and—with its energy-efficient performance—server refreshes.

Learn More

For more information on Intel microarchitecture (Nehalem) including animations and podcasts, visit:
www.intel.com/technology/architecture-silicon/next-gen/index.htm

For more on Intel's 45nm Hi-k metal gate process technology, see: **www.intel.com/technology/45nm**

For more on Intel QuickPath Technology, download the Intel QuickPath Architecture white paper at:
www.intel.com/technology/quickpath

For more on Intel Xeon processor 5500 series, download the product brief at:
www.intel.com/Assets/PDF/prodbrief/xeon-5500.pdf

To learn more about Intel Xeon processor 3500 series, visit:
www.intel.com/p/en_US/products/server/processor/xeon3000

For more on Intel SSE4, download the white paper, "Extending the World's Most Popular Processor Architecture," at:
download.intel.com/technology/architecture/new-instructions-paper.pdf

www.intel.com

[1] Hyper-Threading Technology requires a computer system with a processor supporting Hyper-Threading Technology and an HT Technology enabled chipset, BIOS and operating system. Performance will vary depending on the specific hardware and software you use. See www.intel.com/info/hyperthreading/ for more information including details on which processors support HT Technology.

[2] Intel internal measurement. (Feb 2009) Stream-Triad benchmark. Red Hat Enterprise Linux Server 5.3. Intel® Xeon® processor E5472, 3.0 GHz, 2x6 MB L2 cache, 1600 MHz system bus, 16 GB memory (8x2 GB FB DDR2-800) vs. Intel® Xeon® processor X5570, 2.93 GHz, 8 MB L3 cache, 6.4QPI, 24 GB memory (6x4 GB DDR3-1333).

[3] Not applicable to Macintosh operating systems. Uses Intel® Turbo Boost Technology which requires a platform with a processor with Intel Turbo Boost Technology capability. Intel Turbo Boost Technology performance varies depending on hardware, software and overall system configuration. Check with your platform manufacturer on whether your system delivers Intel Turbo Boost Technology. For more information, see www.intel.com/technology/turboboost.

[4] Intel® Virtualization Technology requires a computer system with an enabled Intel® processor, BIOS, virtual machine monitor (VMM) and, for some uses, certain platform software enabled for it. Functionality, performance or other benefits will vary depending on hardware and software configurations and may require a BIOS update. Software applications may not be compatible with all operating systems. Please check with your application vendor.

[5] Performance results on VMmark benchmark. Intel® Xeon processor X5470 data based on published results. Intel® Xeon processor X5570 Intel internal measurement. (Feb 2009): HP Proliant ML370 G5 server platform with Intel Xeon processors X5470 3.33 GHz, 2x6 MB L2 cache, 1333 MHz FSB, 48 GB memory, VMware* ESX* V3.5.0 Update 3 Published at 9.15@ 7 tiles vs. Intel® Xeon® processor X5570, 2.93 GHz, 8 MB L3 cache, 6.4QPI, 72 GB memory (18x4 GB DDR3-800), VMware* ESX* Build 140815. Performance measured at 19.51@ 13 tiles.

[6] For a more in-depth discussion of how Intel Turbo Boost technology works, see: http://download.intel.com/design/processor/applnots/320354.pdf

[7] Depending on processor SKU.

[8] Intel internal measurement. (April 2008) Ixia* IxChariot* 6.4 benchmark. VMWare* ESX* v3.5U1. Intel® Xeon® processor E5355, 2.66 GHz, 8 MB L2 cache, 1333 MHz system bus, 8 GB memory (8x1 GB FB DIMM 667 MHz).

All products, platforms, dates, and figures specified are preliminary based on current expectations, and are subject to change without notice.

All data is based on comparisons of engineering data sheets or measurements using actual hardware or simulators.

Intel® Virtualization Technology requires a computer system with an enabled Intel® processor, BIOS, virtual machine monitor (VMM) and, for some uses, certain platform software enabled for it. Functionality, performance or other benefits will vary depending on hardware and software configurations and may require a BIOS update. Software applications may not be compatible with all operating systems. Please check with your application vendor.

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