This chapter provides guidelines to improve your system’s signal integrity and to successfully implement an LPDDR2 SDRAM interface in your system.

The LPDDR2 SDRAM Controller with UniPHY intellectual property (IP) enables you to implement LPDDR2 SDRAM interfaces with Arria® V and Cyclone® V devices. This chapter focuses on the following key factors that affect signal integrity:

- I/O standards
- LPDDR2 configurations
- Signal terminations
- Printed circuit board (PCB) layout guidelines

**I/O Standards**

LPDDR2 SDRAM interface signals use HSUL-12 JEDEC I/O signaling standards, which provide low power and low emissions. The HSUL-12 JEDEC I/O standard is mainly for point-to-point unterminated bus topology. This standard eliminates the need for external series or parallel termination resistors in LPDDR2 SDRAM implementation. With this standard, termination power is greatly reduced and programmable drive strength is used to match the impedance.

To select the most appropriate standard for your interface, refer to the Device Datasheet for Arria V Devices chapter in the Arria V Device Handbook, or the Device Datasheet for Cyclone V Devices chapter in the Cyclone V Device Handbook.
LPDDR2 SDRAM Configurations

The LPDDR2 SDRAM Controller with UniPHY IP supports interfaces for LPDDR2 SDRAM with a single device, and multiple devices up to a maximum width of 32 bits.

When using multiple devices, a balanced-T topology is recommended for the signal connected from single point to multiple point, to maintain equal flight time.

You should connect a 200 ohm differential termination resistor between CK/CK# in multiple device designs as shown in Figure 6–2, to maintain an effective resistance of 100 ohms.

You should also simulate your multiple device design to obtain the optimum drive strength settings and ensure correct operation.

Figure 6–1 shows the main signal connections between the FPGA and a single LPDDR2 SDRAM component.

Figure 6–1. Configuration with a Single LPDDR2 SDRAM Component

Notes to Figure 6–1:

1. Use external discrete termination, as shown for CKE, but you may require a pull-down resistor to GND. Refer to the LPDDR2 SDRAM device data sheet for more information about LPDDR2 SDRAM power-up sequencing.
Figure 6–2 shows the differential resistor placement for CK/CK# for multi-point designs.

**Figure 6–2. CK Differential Resistor Placement for Multi Point Design**

Notes to Figure 6–2:

1. Place 200-ohm differential resistors near the memory devices at the end of the last board trace segments.
Figure 6–3 shows the detailed balanced topology recommended for the address and command signals in the multi-point design.

**Figure 6–3. Address Command Balanced-T Topology**

![Figure 6–3 diagram]

**Notes for Figure 6–3:**
1. Split the trace close to the memory devices to minimize signal reflections and impedance nonuniformity.
2. Keep the TL2 traces as short as possible, so that the memory devices appear as a single load.

### Signal Terminations

Arria V and Cyclone V devices offer OCT technology. Table 6–1 lists the extent of OCT support for each device.

**Table 6–1. On-Chip Termination Schemes**

<table>
<thead>
<tr>
<th>Termination Scheme</th>
<th>I/O Standard</th>
<th>Arria V and Cyclone V</th>
</tr>
</thead>
<tbody>
<tr>
<td>On-Chip Series Termination without Calibration</td>
<td>HSUL-12</td>
<td>34/40/48/60/80</td>
</tr>
<tr>
<td>On-Chip Series Termination with Calibration</td>
<td>HSUL-12</td>
<td>34/40/48/60/80</td>
</tr>
</tbody>
</table>

On-chip series (R<sub>o</sub>) termination supports output buffers, and bidirectional buffers only when they are driving output signals. LPDDR2 SDRAM interfaces have bidirectional data paths. The UniPHY IP uses series OCT for memory writes but no parallel OCT for memory reads because Arria V and Cyclone V support only on-chip series termination in the HSUL-12 I/O standard.

For Arria V and Cyclone V devices, the HSUL-12 I/O calibrated terminations are calibrated against 240 ohm 1% resistors connected to the R<sub>ZQ</sub> pins in an I/O bank with the same V<sub>CCIO</sub> as the LPDDR2 interface.

Calibration occurs at the end of the device configuration.
LPDDR2 SDRAM memory components have a ZQ pin which connects through a resistor \( R_{ZQ} \) (240 ohm) to ground. The output signal impedances for LPDDR2 SDRAM are 34.3 ohm, 40 ohm, 48 ohm, 60 ohm, 80 ohm, and 120 ohm. The output signal impedance is set by mode register during initialization. Refer to the LPDDR2 SDRAM device data sheet for more information.

For information about OCT, refer to the *I/O Features in Arria V Devices* chapter in the *Arria V Device Handbook*, or the *I/O Features in Cyclone V Devices* chapter in the *Cyclone V Device Handbook*.

The following section shows HyperLynx simulation eye diagrams to demonstrate signal termination options. Altera strongly recommends signal terminations to optimize signal integrity and timing margins, and to minimize unwanted emissions, reflections, and crosstalk.

All of the eye diagrams shown in this section are for a 50 ohm trace with a propagation delay of 509 ps which is approximately a 2.8-inch trace on a standard FR4 PCB. The signal I/O standard is HSUL-12.

The eye diagrams in this section show the best case achievable and do not take into account PCB vias, crosstalk, and other degrading effects such as variations in the PCB structure due to manufacturing tolerances.

Simulate your design to ensure correct operation.

### Outputs from the FPGA to the LPDDR2 Component

The following output signals are from the FPGA to the LPDDR2 SDRAM component:

- write data (\( \text{DQ} \))
- data mask (\( \text{DM} \))
- data strobe (\( \text{DQS/DQS#} \))
- command address
- command (\( \text{CS}, \text{and CKE} \))
- clocks (\( \text{CK/CK#} \))

No far-end memory termination is needed when driving output signals from FPGA to LPDDR2 SDRAM. Cyclone V and Arria V devices offer the OCT series termination for impedance matching.

The HyperLynx simulation eye diagrams show simulation cases of write data, address, and chip-select signals with the OCT settings. All eye diagrams are shown at the connection to the receiver device die.
Figure 6–4 shows the double data rate write data using an Arria V HSUL-12 with calibrated series 34 ohm OCT output driver.

Figure 6–4. Write Data Simulation at 400 MHz
Figure 6–5 shows an address command signal at a frequency of 400 MHz using Arria V HSUL-12 with calibrated series 34 ohm OCT. Address command signals are also double data rate so they are running at 400 MHz.

**Figure 6–5. Address Command at 400 MHz Termination**
Figure 6–6 shows a memory clock signal at a frequency of 400 MHz using Arria V HSUL-12 with calibrated series 34 ohm OCT.

**Figure 6–6. Memory Clock Simulation at 400MHz**

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**Input to the FPGA from the LPDDR2 SDRAM Component**

The LPDDR2 SDRAM component drives the following input signals into the FPGA:

- read data
- DQS

LPDDR2 SDRAM provides the flexibility to adjust drive strength to match the impedance of the memory bus, eliminating the need for termination voltage (VTT) and series termination resistors.

The programmable drive strength options are 34.3 ohms, 40 ohms (default), 48 ohms, 60 ohms, 80 ohms, and 120 ohms. You must perform board simulation to determine the best option for your board layout.

By default, Altera LPDDR2 SDRAM UniPHY IP uses 40 ohm drive strength.

The eye diagrams are shown at the FPGA die pin, and the LPDDR2 SDRAM output driver is HSUL-12 with ZQ calibration of 40 ohms. The LPDDR2 SDRAM read data is double data rate.
Figure 6–7 shows read data simulation at 400 MHz with 40 W drive strength on an Arria V device.

Figure 6–7. Read Data Simulation at 400 MHz with 40 Ω Drive Strength on an Arria V Device

Termination Schemes

Table 6–2 lists the recommended termination schemes for major LPDDR2 SDRAM memory interface signals, which include data (DQ), data strobe (DQS), data mask (DM), clocks (CK, and CK#), command address (CA), and control (CS#, and CKE).

Table 6–2. Termination Recommendations for Arria V and Cyclone V Devices (Part 1 of 2)

<table>
<thead>
<tr>
<th>Signal Type</th>
<th>HSUL-12 Standard (1), (2)</th>
<th>Memory End Termination</th>
</tr>
</thead>
<tbody>
<tr>
<td>DQS/DQS#</td>
<td>R34 CAL</td>
<td>ZQ40</td>
</tr>
<tr>
<td>Data (Write)</td>
<td>R34 CAL</td>
<td>–</td>
</tr>
<tr>
<td>Data (Read)</td>
<td>–</td>
<td>ZQ40</td>
</tr>
<tr>
<td>Data Mask (DM)</td>
<td>R34 CAL</td>
<td>–</td>
</tr>
<tr>
<td>CK/CK# Clocks</td>
<td>R34 CAL</td>
<td>(\times 1 = – (4))</td>
</tr>
<tr>
<td>Command Address (CA)</td>
<td>R34 CAL</td>
<td>(\times 2 = 200 \Omega) Differential (5)</td>
</tr>
<tr>
<td>Chip Select (CS#)</td>
<td>R34 CAL</td>
<td>–</td>
</tr>
</tbody>
</table>
### The recommended termination schemes of Table 6–2 are based on 2.8 inch maximum trace length analysis. You may add the external termination resistor or adjust the drive strength to improve signal integrity for longer trace lengths. Recommendations for external termination are as follows:

- **Class I termination (50 ohms parallel to VTT at the memory end)** — Unidirectional signal (Command Address, control, and CK/CK# signals)
- **Class II termination (50 ohms parallel to VTT at both ends)** — Bidirectional signal (DQ and DQS/DQS# signal)

Altera recommends that you simulate your design to ensure good signal integrity.

### PCB Layout Guidelines

Table 6–3 lists the LPDDR2 SDRAM general routing layout guidelines.

The following layout guidelines include several +/- length-based rules. These length-based guidelines are for first order timing approximations if you cannot simulate the actual delay characteristics of your PCB implementation. They do not include any margin for crosstalk.

Altera recommends that you get accurate time base skew numbers when you simulate your specific implementation.

### Table 6–2. Termination Recommendations for Arria V and Cyclone V Devices (Part 2 of 2)

<table>
<thead>
<tr>
<th>Signal Type</th>
<th>HSUL-12 Standard (1), (2)</th>
<th>Memory End Termination</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Enable (CKE)</td>
<td>R34 CAL</td>
<td>4.7 KΩ parallel to GND</td>
</tr>
</tbody>
</table>

**Notes to Table 6–2:**

1. R is effective series output impedance.
2. CAL is OCT with calibration.
3. Altera recommends that you use a 4.7 KΩ parallel to GND if your design meets the power sequencing requirements of the LPDDR2 SDRAM component. Refer to the LPDDR2 SDRAM data sheet for further information.
4. ×1 is a single-device load.
5. ×2 is a double-device load. An alternative option is to use a 100 Ω differential termination at the trace split.

### Table 6–3. LPDDR2 Layout Guidelines (Part 1 of 3)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Guidelines</th>
</tr>
</thead>
</table>
| Impedance         | All signal planes must be 50 Ω single-ended, ±10%.
|                   | All signal planes must be 100 Ω differential ±10%.
|                   | Remove all unused via pads, because they cause unwanted capacitance. |
| Decoupling Parameter | Use 0.1 μF in 0402 size to minimize inductance. |
|                   | Verify your capacitive decoupling using the Altera Power Distribution Network (PDN) Design tool. |
| Power             | Route GND, 1.2 V and 1.8 V as planes. |
|                   | Route VCCIO for memories in a single split plane with at least a 20-mil (0.020 inches or 0.508 mm) gap of separation. |
|                   | Route oscillators and PLL power as islands or 100-mil (2.54-mm) power traces. |
Table 6–3. LPDDR2 Layout Guidelines (Part 2 of 3)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Guidelines</th>
</tr>
</thead>
</table>
| General Routing | - All specified delay matching requirements include PCB trace delays, different layer propagation, velocity variance, and crosstalk. To minimize PCB layer propagation variance, Altera recommends that signals from the same net group always be routed on the same layer. If you must route signals of the same net group on different layers with the same impedance characteristic, simulate your worst case PCB trace tolerances to ascertain actual propagation delay differences. Typical layer to layer trace delay variations are of 15 ps/inch order.  
  - Use 45° angles (not 90° corners).  
  - Avoid T-Junctions for critical nets or clocks.  
  - Avoid T-junctions greater than 75 ps (approximately 25 mils, 6.35 mm).  
  - Disallow signals across split planes.  
  - Restrict routing other signals close to system reset signals.  
  - Avoid routing memory signals closer than 0.025 inch (0.635 mm) to PCI or system clocks.  
  - Match all signals within a given DQ group with a maximum skew of ±10 ps or approximately ±50 mils (0.254 mm) and route on the same layer. |
| Clock Routing | - Route clocks on inner layers with outer-layer run lengths held to under 150 ps (approximately 500 mils, 12.7 mm).  
  - These signals should maintain a 10-mil (0.254 mm) spacing from other nets.  
  - Clocks should maintain a length-matching between clock pairs of ±5 ps or approximately ±25 mils (0.635 mm).  
  - Differential clocks should maintain a length-matching between P and N signals of ±2 ps or approximately ±10 mils (0.254 mm).  
  - Space between different clock pairs should be at least three times the space between the traces of a differential pair. |
| Address and Command Routing | - To minimize crosstalk, route address, and command signals on a different layer than the data and data mask signals.  
  - Do not route the differential clock (CK/CK#) and clock enable (CKE) signals close to the address signals. |
Altera recommends the following layout approach, based on the layout guidelines in Table 6–3:

1. Route the differential clocks (CK/CK#) and data strobe (DQS/DQS#) with a length-matching between P and N signals of ±2 ps.
2. Route the DQS/DQS# associated with a DQ group on the same PCB layer. Match these DQS pairs to within ±5 ps.
3. Set the DQS/DQS# as the target trace propagation delay for the associated data and data mask signals.
4. Route the data and data mask signals for the DQ group ideally on the same layer as the associated DQS/DQS# to within ±10 ps skew of the target DQS/DQS#.
5. Route the CK/CK# clocks and set as the target trace propagation delays for the DQ group. Match the CK/CK# clock to within ±50 ps of all the DQS/DQS#.
6. Route the address/control signal group (address, CS, CKE) ideally on the same layer as the CK/CK# clocks, to within ±20 ps skew of the CK/CK# traces.

This layout approach provides a good starting point for a design requirement of the highest clock frequency supported for the LPDDR2 SDRAM interface.

Altera recommends that you create your project in the Quartus® II software with a fully implemented LPDDR2 SDRAM Controller with UniPHY interface, and observe the interface timing margins to determine the actual margins for your design.
Although the recommendations in this chapter are based on simulations, you can apply the same general principles when determining the best termination scheme, drive strength setting, and loading style to any board designs. Even armed with this knowledge, it is still critical that you perform simulations, either using IBIS or HSPICE models, to determine the quality of signal integrity on your designs.

Document Revision History

Table 6–4 lists the revision history for this document.

Table 6–4. Document Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>November 2012</td>
<td>1.0</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>