High-Performance, High-Density FPGAs

Introducing Stratix® II devices—the latest in high-density, high-performance FPGAs from Altera. Built on a new and innovative logic structure, Stratix II devices on average deliver 50 percent faster performance and offer more than twice the logic capacity of prior-generation FPGAs. Benchmarking results have shown that Stratix II FPGAs deliver the highest performance of any other competing FPGA. Stratix II devices support internal clock frequency rates of up to 500 MHz and typical design performance at over 250 MHz. The new logic structure allows designers to pack significantly more functionality into less area, further reducing product costs. This means that designers can now get ASIC-like density and performance with the time-to-market advantages of implementing their designs with programmable logic. Stratix II devices eliminate the performance-density-cost barriers that have forced designers to use time-consuming alternative technologies.

Optimized for the 90-nm process technology node, these second-generation devices include all of the features and characteristics of the award-winning Stratix FPGA family.

Costing approximately 40 percent less than Stratix devices for equivalent densities, Stratix II devices give customers an optimal solution for medium- to high-volume applications.

For higher-volume applications, HardCopy® structured ASICs for Stratix II FPGAs offer the industry’s only seamless development path from FPGA prototype to high-volume, low-cost production. The HardCopy structured ASIC version of the Stratix II FPGA design further increases performance and reduces power consumption over the FPGA implementation and offers significantly lower unit costs.

Stratix II devices are supported in Quartus® II software, the industry’s most advanced development software for high-density FPGA designs. Developed with many new ASIC-like design capabilities, Quartus II software provides customers with a comprehensive suite of synthesis, optimization, and verification tools in a single, unified design environment. Timing closure and block-based design methodologies and features such as SOPC Builder and the SignalTap® II logic analyzer moves designs from concept to production in hours.

<table>
<thead>
<tr>
<th>Table 1. Stratix II Family Highlights</th>
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<tbody>
<tr>
<td>Feature</td>
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</table>
| New Logic Structure                 | Based on a new, innovative logic structure consisting of adaptive logic modules (ALMs) that delivers higher performance and maximum resource efficiency. Includes dedicated functionality to efficiently implement adder trees and other complex arithmetic functions.
| High-Performance Logic Array        | Stratix II devices support internal clock rates of up to 500 MHz with typical system performance in excess of 250 MHz. The average performance of Stratix II devices is 50 percent higher than first-generation Stratix devices.
| External Memory Interface Circuitry | Support for the latest external memory interfaces in dedicated circuitry, including 267-MHz DDR2 SDRAM, 300-MHz RLDRAM II, and 200-MHz QDRII SRAM devices with sufficient bandwidth and I/O pins to support interfacing with multiple, standard 64-bit, 168-/144-pin dual in-line memory modules (DIMMs).
| 1-Gbps Differential I/O & High-Speed Interfaces | Support for high-speed I/O standards and high-speed interfaces such as 10-Gigabit Ethernet (XSBII), SFI-4, SPI 4.2, HyperTransport™, RapidIO™, and UTOPIA Level 4 interfaces at up to 1 Gbps.
| Dynamic Phase Alignment (DPA)       | Maximizes signal integrity and simplifies printed circuit board (PCB) layout and timing management for high-speed data transfer. Enables 1-Gbps data transfer rates by eliminating channel-to-channel and channel-to-clock skew in high-speed data transmission systems.
| TriMatrix™ Memory                   | Up to 9 Mbits of memory in three block sizes with parity, capable of up to 370-MHz performance.                                                              |
| DSP Blocks                          | Optimized to meet the performance need of high-speed DSP applications such as JPEG2000, MPEG-4, 802.11x, wideband code division multiple access (W-CDMA), high-speed downlink packet access (HSDPA), and 1x EV DO. The DSP blocks offer up to 384 18x18 multipliers that operate at up to 370 MHz.
| Design Security                     | 128-bit AES encryption technology and non-volatile key storage for preventing intellectual property (IP) theft.
| Clock Management Circuitry         | Up to 12 phase-locked loops (PLLs) and up to 48 system clocks—with features such as PLL reconfiguration, spread-spectrum clocking, frequency synthesis, programmable phase shift, and delay shift for all on- and off-chip clocking requirements.
| Remote System Upgrades             | Enables reliable, safe deployment of in-system upgrades and bug fixes.                                                                                       |
| HardCopy Support for Stratix II Devices | A seamless, cost-reduction migration path to low-cost HardCopy structured ASICs.                                                                                   |
Setting the Standard in FPGA Technology

Based on the highly acclaimed Stratix device family’s features—such as TriMatrix memory, digital signal processing (DSP) blocks, and external memory interfaces—Stratix II devices set new standards for FPGA technology. Stratix II FPGAs are manufactured on a 1.2-V, 90-nm, all-layer-copper SRAM process, with densities ranging from 15,600 to 179,400 equivalent logic elements (LEs) and up to 9 Mbits of embedded RAM. New to Stratix II devices are features such as design security that uses 128-bit advanced encryption standard (AES) and non-volatile key storage, DPA circuitry, and support for new external memory interfaces. Table 1 highlights the features and benefits of Stratix II devices, and Table 2 shows the wide range of the features and packages available.

Innovative Stratix II Architecture

The Stratix II architecture was designed with performance in mind. Starting with its innovative logic structure that is constructed with Altera’s new adaptive logic modules (ALMs), Stratix II FPGAs take device logic efficiency and internal frequencies to never-before-seen levels. See Figure 1 for a depiction of the Stratix II floorplan.

### Table 2. Stratix II Family Highlights

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>Adaptive Logic Modules(^1)</td>
<td>6,240</td>
<td>13,552</td>
<td>24,176</td>
<td>36,384</td>
<td>53,016</td>
<td>71,760</td>
</tr>
<tr>
<td>Equivalent Logic Elements</td>
<td>15,600</td>
<td>33,880</td>
<td>60,440</td>
<td>90,960</td>
<td>132,540</td>
<td>179,400</td>
</tr>
<tr>
<td>MS12 RAM Blocks (512 bits + parity)</td>
<td>104</td>
<td>202</td>
<td>329</td>
<td>488</td>
<td>699</td>
<td>930</td>
</tr>
<tr>
<td>M4K RAM Blocks (4 Kbits + parity)</td>
<td>78</td>
<td>144</td>
<td>255</td>
<td>408</td>
<td>609</td>
<td>768</td>
</tr>
<tr>
<td>M-RAM Blocks (512 Kbits + parity)</td>
<td>0</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>6</td>
<td>9</td>
</tr>
<tr>
<td>Total RAM Bits</td>
<td>419,328</td>
<td>1,369,728</td>
<td>2,544,192</td>
<td>4,520,448</td>
<td>6,747,840</td>
<td>9,383,040</td>
</tr>
<tr>
<td>DSP Blocks(^2)</td>
<td>12</td>
<td>16</td>
<td>36</td>
<td>48</td>
<td>63</td>
<td>96</td>
</tr>
<tr>
<td>Embedded 18-bit x 18-bit Multipliers</td>
<td>48</td>
<td>64</td>
<td>144</td>
<td>192</td>
<td>252</td>
<td>384</td>
</tr>
<tr>
<td>PLLs</td>
<td>6</td>
<td>6</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td>Maximum User I/O Pins</td>
<td>366</td>
<td>500</td>
<td>718</td>
<td>902</td>
<td>1,126</td>
<td>1,170</td>
</tr>
<tr>
<td>Available Packages</td>
<td>484-Pin FBGA(^3), 672-Pin FBGA</td>
<td>484-Pin FBGA, 672-Pin FBGA</td>
<td>484-Pin FBGA, 672-Pin FBGA, 1,020-Pin FBGA</td>
<td>484-Pin HFBGA(^4), 780-Pin FBGA, 1,020-Pin FBGA, 1,508-Pin FBGA</td>
<td>780-Pin FBGA, 1,020-Pin FBGA, 1,508-Pin FBGA</td>
<td>1,020-Pin FBGA, 1,508-Pin FBGA</td>
</tr>
</tbody>
</table>

Notes:
\(^1\) Each ALM is equivalent to 2.5 4-input LUT-based logic elements
\(^2\) 4 18-bit x 18-bit multipliers per DSP block
\(^3\) FBGA: FineLine BGA package
\(^4\) HFBGA: Hybrid FineLine BGA package. The 484-Pin HFBGA has a body size of 27mm x 27mm.
New Logic Structure
The new and innovative ALMs in Stratix II devices deliver more logic capacity and faster performance in a smaller physical area. The Stratix II architecture significantly reduces the logic resources required to implement any given function and the number of logic levels in a given critical path. The architecture accomplishes this by permitting inputs to be shared by adjacent look-up tables (LUTs) in the same ALM. Multiple, independent functions can also be packed into a single ALM, further reducing logic resource requirements. This is important at the 90-nm node where interconnect delay assumes a larger proportion of the total FPGA delay and where reducing interconnect traversals becomes crucial to maximizing device performance. Figure 2 diagrams a Stratix II ALM.

Design Security
As FPGA designs become increasingly complex and begin to assume critical roles in system functionality, IP theft can be a concern. To provide designers with a secure means to protect their systems, Stratix II devices are designed with AES encryption technology and non-volatile key storage. As shown in Figure 3, each Stratix II device can be securely configured with an encrypted configuration file generated by Quartus II software and stored in an external configuration device.

High-Bandwidth I/O Standards & High-Speed Interfaces
FPGAs have become an integral part of virtually all digital systems and must be able to communicate with a variety of devices. Stratix II FPGAs support many single-ended and differential I/O standards for interfacing with anything from backplanes, host processors, buses, and memory devices to 3D graphics controllers.

Source-Synchronous Signaling With DPA
Stratix II devices give designers access to up to 156 receiver and 156 transmitter high-speed differential channels capable of 1-Gbps performance. Each of these I/O channels includes dedicated serializer/deserializer (SERDES) and DPA circuitry. The DPA feature can eliminate channel-to-channel skew as well as clock-to-channel skew, as shown in Figure 4 on page 5. This improves the reliability of bandwidth-intensive data transfers and simplifies the complexity associated with implementing high-speed interface standards such as the 10 Gigabit Ethernet XSBI, SFI-4, SPI-4.2, HyperTransport, RapidIO, and CSIX standards.

Single-Ended I/O Standard Support
Stratix II devices support single-ended I/O standards such as LVTTL, LVCMOS, SSTL, HSTL, peripheral component interconnect (PCI), and PCI-X. Single-ended I/O standards provide more current drive capacity than differential I/O standards, necessary when designing with advanced memory devices such as double data rate 2 (DDR2) SDRAM and quad data rate II (QDRII) SRAM devices.

High-Speed External Memory Interface Support
In addition to the abundant on-chip TriMatrix memory, Stratix II devices provide customers with dedicated external memory interfaces for memory-intensive design requirements. Designers can easily connect Stratix II devices to a wide range of the latest standard SRAM and DRAM memory devices, as shown in Table 3 on page 5. Using Stratix II device features and customizable IP, designers can integrate high-density memory devices into complex system designs without reducing data-access performance or increasing development time.
Altera Corporation

High-Performance Memory Bandwidth

Stratix II FPGAs utilize the TriMatrix memory structure, pioneered in Stratix devices. TriMatrix memory includes 512-bit M512 blocks, 4-Kbit M4K blocks, and 512-Kbit M-RAM blocks, each of which can be configured to support a wide range of features. Each embedded RAM block in the TriMatrix memory structure targets a different class of applications: the M512 blocks can be used for small functions such as first-in first-out (FIFO) applications, the M4K blocks can be used to store incoming data from multi-channel I/O protocols, and the M-RAM blocks can be used for storage-intensive applications such as Internet protocol packet buffering or program/data memory for an on-chip Nios® II embedded processor. All memory blocks include extra parity bits for error control, embedded shift register functionality, mixed-width mode, and mixed-clock mode support. Additionally, the M4K and M-RAM blocks support true dual-port mode and byte masking for advanced write operations. With up to 9 Mbits of RAM and a 370 MHz maximum clock speed, the TriMatrix memory structure, shown in Figure 5, makes the Stratix II device family an ideal choice for memory-intensive applications.

Table 3. Stratix II Memory Interface Support

<table>
<thead>
<tr>
<th>Interface</th>
<th>Maximum Clock Frequency (MHz)</th>
<th>Maximum Data Rate (Mbps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDR SDRAM</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>DDR SDRAM</td>
<td>200</td>
<td>400</td>
</tr>
<tr>
<td>DDR2 SDRAM</td>
<td>267</td>
<td>533</td>
</tr>
<tr>
<td>RLDRII SDRAM</td>
<td>300</td>
<td>600</td>
</tr>
<tr>
<td>QDRII SRAM</td>
<td>250</td>
<td>1,000</td>
</tr>
</tbody>
</table>

Unmatched DSP Horsepower

Stratix II DSP blocks are optimized to implement processing-intensive functions such as filtering, compression, chip-rate processing, equalization, digital intermediate frequency, transforms, and modulation. Using DSP blocks, Stratix II FPGAs can easily meet the DSP throughput requirements of emerging standards and protocols such as JPEG2000, MPEG-4, 802.11x, code-division multiple access 2000 (CDMA2000), 1x EV DV, HSDP, and W-CDMA. Capable of running at 370 MHz, Stratix II DSP blocks provide maximum DSP throughput (up to 284 GMACs) that is orders of magnitude higher than leading-edge digital signal processors available today.

Each DSP block can support a variety of multiplier bit sizes (9x9, 18x18, 36x36) and operation modes (multiplication, complex multiplication, multiply-accumulate, and multiply-add), and can generate DSP throughput of 3.0 GMACS per DSP block.

In addition, rounding and saturation support has been added to the DSP block to facilitate the porting of DSP firmware code onto FPGA designs. Many applications, such as speech processing, use rounding and saturation due to the fixed widths of the memory buffers that store the data. In the past, DSP designers using fixed-point numbers had to modify their design to accommodate rounding and saturation. With the rounding and saturation support in DSP blocks, it...
is now much easier to port digital signal processor-based designs to FPGA implementations. Figure 6 shows the Stratix II DSP block circuitry.

**Enhanced System Clock Management**

With up to 12 PLLs and up to 48 system clocks per device, Stratix II FPGAs are built to function as the central clock manager for meeting system timing challenges. These PLLs feature system-level clock management features usually found only in high-end discrete PLL devices. Stratix II devices provide two types of PLLs: enhanced and fast PLLs. Enhanced PLLs support advanced features such as external feedback, clock switchover, PLL reconfiguration, spread-spectrum clocking, and programmable bandwidth. Fast PLLs are optimized for high-speed differential I/O interfaces but can be used for general-purpose clocking. Figure 7 illustrates the system timing features of Stratix II PLLs.

**On-Chip Termination**

As today’s system speeds and clock edge rates steadily increase, signal integrity has become crucial in digital designs. To improve signal integrity, both single-ended and differential signals should be properly terminated. Termination can be implemented with external termination resistors on a board or with on-chip termination technology. Stratix II devices provide on-chip termination that supports both series and differential termination schemes.

**Remote System Upgrades**

Using FPGAs gets designs to market faster, and customers utilizing the remote system upgrade capability in Stratix II devices can keep their products on technology’s cutting edge longer. Remote system upgrades can be transmitted through any communications network to keep a customer’s design updated and to prolong a product’s lifecycle. Stratix II devices provide superior design flexibility and extended product life, as shown in Figure 8.
**Altera SOPC Solutions**

Altera offers a total solution for creating system-on-a-programmable-chip (SOPC) solutions on Stratix II devices, including Quartus II design software, optimized IP, the Nios II embedded processor, and customer training.

**Design Software Technology Leadership**

Realize the full potential of Stratix II designs using Quartus II software. Altera’s powerful yet easy-to-use design software now features unique advantages in design flow methodology support; system design, IP integration, and IP evaluation; place-and-route technology; timing closure methodology; in-system verification technology; and third-party EDA support. Quartus II software provides the most comprehensive environment available for FPGA, CPLD, and HardCopy structured ASIC designs. Quartus II software technology leadership and the Stratix II device family deliver designers unmatched performance, efficiency, and ease-of-use for high-density FPGA designs. For details on Quartus II software, refer to [www.altera.com/quartus2](http://www.altera.com/quartus2).

**Broadest Portfolio of Intellectual Property**

Altera® and Altera Megafunction Partners Program (AMPP℠) partners offer off-the-shelf IP cores optimized for Stratix II devices, along with an extensive library of standard IP cores. IP cores provide total solutions by targeting specific application areas, improving performance and system reusability, and significantly reducing a product’s time-to-market. Visit the IP MegaStore (on the Altera® web site at [www.altera.com/ipmegastore](http://www.altera.com/ipmegastore)) to try out and to purchase IP.

**Complete Nios II Embedded Processor Solutions**

The Nios II family of embedded processors features a general-purpose RISC CPU architecture designed to address a wide range of embedded applications in Altera FPGAs. The Nios II processor family consists of three cores:

- **Nios II/f (fast):** maximum performance
- **Nios II/s (standard):** balanced performance and size
- **Nios II/e (economy):** minimum logic usage

The three Nios II processors share a common 32-bit instruction set architecture and are 100 percent binary-code-compatible.

By taking advantage of the advanced architectural features of the Stratix II device family, Nios II processors deliver increased capabilities and performance of over 200 DMIPS. Using the SOPC Builder design tool in Quartus II software, designers can select from a wide array of IP components, connect them, and automatically generate hardware, software, and simulation models for custom processor implementations. For details on Nios II embedded processors, refer to [www.altera.com/nios2](http://www.altera.com/nios2).

**Comprehensive Customer Training**

Customers interested in learning more about designing quickly and efficiently with Stratix II devices can attend one of Altera’s instructor-led modular training series. This Stratix II device-specific series consists of individual training modules that can be arranged to create custom courses tailored to our customers’ needs and experience. Altera also offers three one-day courses that cover all modules. For details visit [www.altera.com/training](http://www.altera.com/training).

**Contact Altera Today**

Get your next high-performance design started today. Visit the Altera web site to learn more about the Stratix II device family and its high-bandwidth solutions at [www.altera.com/stratix2](http://www.altera.com/stratix2).