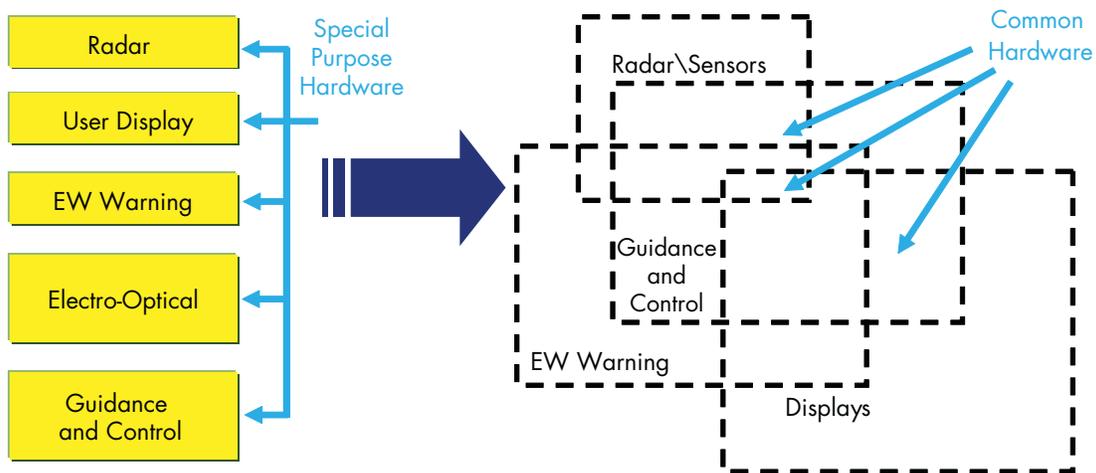


Electronic Warfare Design With PLDs and High-Speed Transceivers

Introduction

Electronic warfare has become part of the strategic landscape for all warfighters on the ground, at sea, and in the air. Threats change quickly, so fast characterization of the electromagnetic landscape and shifting tactical responses are the metrics in modern electronic warfare. This drives the design of reconfigurable logic and software-based systems in military hardware (Figure 1). It also means that algorithm development and operational concepts are beginning to dominate weapon and threat-support systems design.

Figure 1. Military Electronics is Evolving to Common Hardware and Design Reuse



As military systems trend towards smaller and more power-efficient implementations, a logical convergence occurs towards fewer common hardware and software blocks (Figure 2). The technology drivers in this trend are reconfigurable hardware, system latency, and portable on-chip intellectual property (IP).

Figure 2. Changes in the Military Hardware Design Flow Caused by Reusability

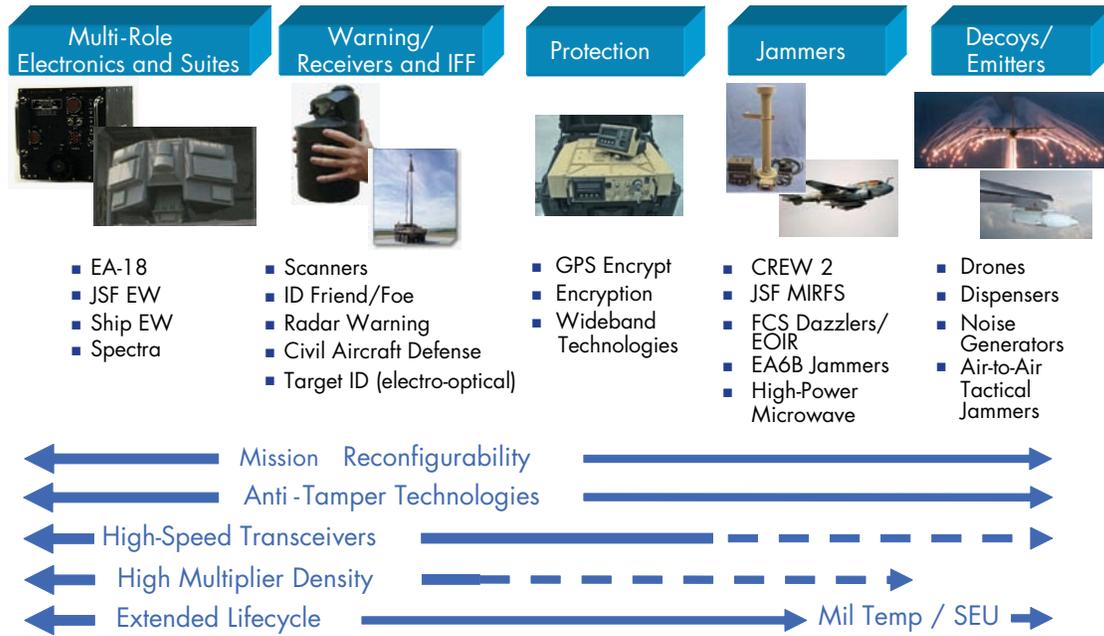


Sharing configurable hardware across systems requires new approaches to electronics designs, and creates new risks in design productivity. Managing and controlling design efforts increasingly challenges the skills of work product managers, and drives them to spend more time examining workflows and selecting the right design tools.

Different Electronic Warfare Requirements

As shown in Figure 3, electronic warfare doctrine divides military electromagnetic activity into electronic support, electronic attack, and electronic protect, and each of these activities is further divided into passive techniques and active ones. This makes the category of electronic warfare span across search, intercept, direction finding, jamming, deception, shielding, encryption, and anti-jam technologies. New commercial and adversary uses of the electromagnetic spectrum appear every year, as does the breadth of usage, thus increasing the territory covered by military systems.

Figure 3. Electronic Warfare Systems With Different Logic Requirements



Electronic warfare activities and devices can be divided roughly into a few smaller categories based on their digital logic requirements. Nearly all benefit from the ability of FPGAs to be reconfigured to update tactics and forestall part obsolescence. Each category of military equipment is also subject to anti-tamper directives to prevent critical design parameters from falling into adversary hands. The digital signal processing (DSP) requirements of many systems drive the need for serial transceivers and hard multipliers. Finally, some missions require extended support cycles, military temperature support, and/or resistance and mitigation for single event upsets (SEUs).

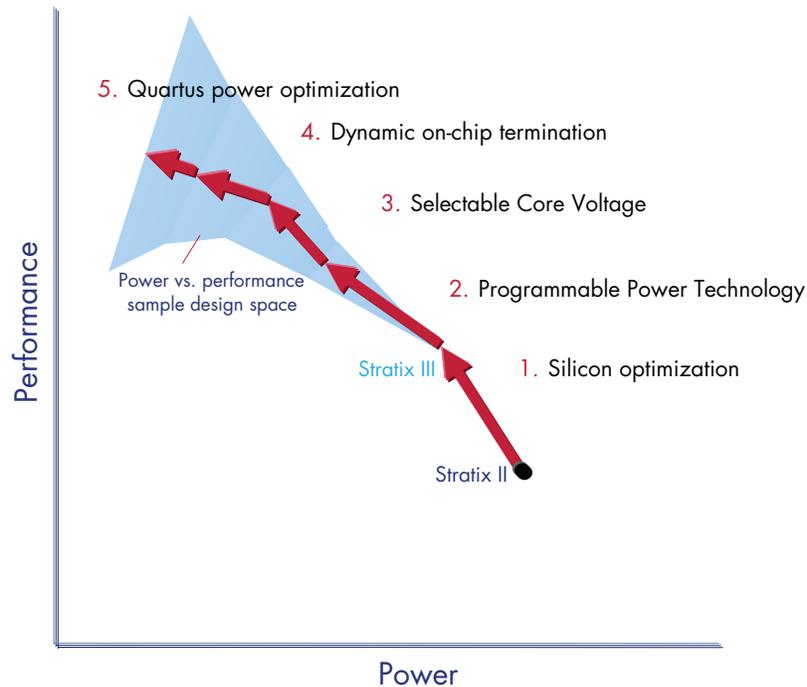
Power and Heat Advantages With FPGAs

Electronic warfare systems have highly variable and unique power and performance requirements, with nearly all military designs bounded by power and heat dissipation. Fortunately, since power and heat are a primary focus for Altera’s FPGA designers, a series of silicon and software power design features has been developed for Stratix® series FPGAs that allow designers to optimize electronics solutions for each mission. Never before have system designers had direct control over the power consumption and heat dissipation of their programmable logic.

The Altera® design flow offers five advantages in allowing the user to select the optimal balance of system power and performance. Altera’s patented Programmable Power Technology allows the designer to channel power to the critical logic path where it is needed, and reduce power where it is not needed. The designer can also select between 0.9V and 1.1V FPGA core voltage, and trade power for performance. Also, Altera’s powerful Quartus II® design software has two new features: the intelligence to terminate unused power connections dynamically, and to optimize power routing in the design.

Using an sample design space as shown in Figure 4, an FPGA designer has the flexibility to tailor an application for both power and performance requirements.

Figure 4. Five Ways to Optimize Military Designs for Power and Performance



Anti-Tamper FPGA Features

Altera programmable logic devices (PLDs) have anti-tamper features that are essential for developing key system-level approaches that protect the system's critical program information (CPI). In addition, Altera has partnerships with White Electronics and several other companies to offer tamper-proof packaging and FPGA sanitization algorithms. For future generations of products, Altera is working with several government agencies to provide advanced anti-tamper capabilities and design features.

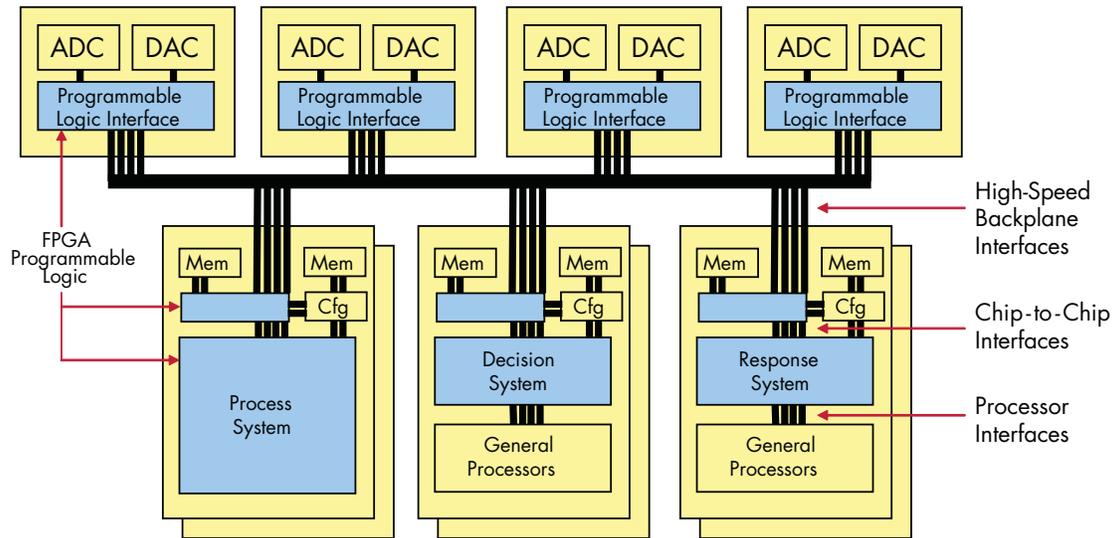
Anti-tamper features in Stratix FPGA designs include a 256-bit AES encryption feature for flash loading of devices with volatile or non-volatile keys. Reference designs are also available for device authentication in a system. Plus, the anti-tamper advantages of the Nios® II embedded processor include compiler uniqueness through multiple instantiations inside any Altera PLD. The opportunity to transition FPGA designs to HardCopy® structured ASICs gives the designer the opportunity to take advantage of the anti-tamper features of an ASIC, in addition to the power and performance advantages over an FPGA.

Open Systems and High-Speed Transceivers

An important initiative in military electronics is the design of “open systems” that use common interface standards and modular command and control, shown in Figure 5. Open systems allow military designers to easily add and remove mission functions without the need to re-engineer all of the subsystems with which it interfaces. True open-system design requires three features in digital logic:

- Reliable high-speed serial transceivers
- Strong IP support libraries of commercial data standards
- System integration tools with high usability

Figure 5. Open Systems Rely on High Speed and Common Interfaces



Transceivers

Altera PLDs have the fastest, most-reliable FPGA transceivers available. With speeds currently specified and characterized up to 6.375 Gbps in Stratix II GX devices and industry-leading signal integrity, open military systems can rely on Altera PLDs to power mission-critical systems. Only Altera has a successful track record of five generations of transceiver devices designed by the same internal design and characterization teams. This reduces risk in product release schedules at Altera, and reduces risk for designers using high-speed serial interfaces.

IP Support

Altera's internal and partner support libraries offer immediate support in PCI-X and PCI Express 1/4/8, SerialRapidIO®, Gigabit Ethernet (GbE), 10G Mac and PCS, Packet over SONET, HyperTransport™, and SerialLite II. More standards are supported every month in Quartus II design software and the SOPC Builder tool.

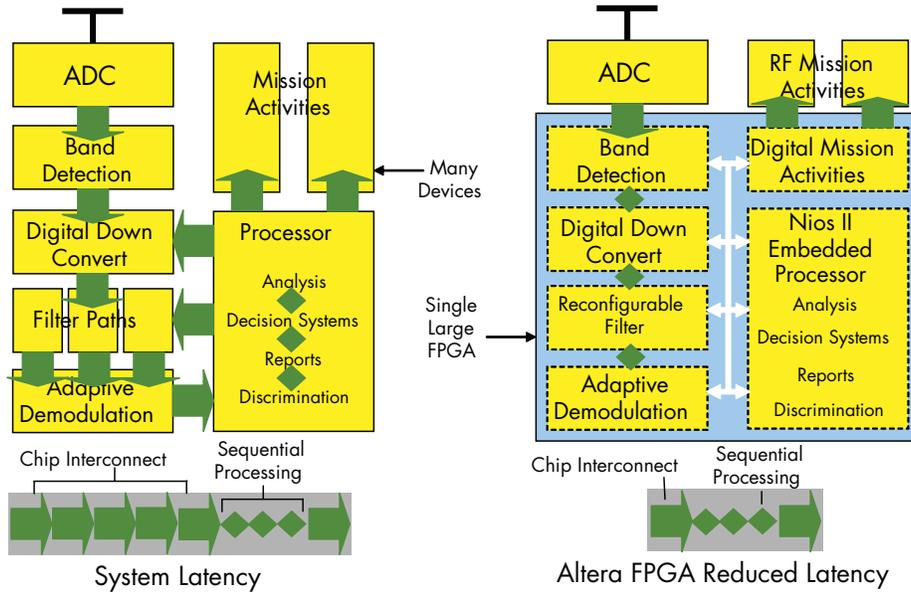
SOPC Builder

The SOPC Builder utility in the Quartus II design suite is designed to take advantage of the open systems philosophy of military systems. Using the common Avalon® interface, IP blocks are easily connected to maximize logic reuse and simplify interconnect tasks. SOPC Builder allows the user to use common logic block interfaces throughout an entire design.

Reducing System Latency With SOPC

By taking advantage of Altera's high-density FPGA families, interconnect and sequential processing latencies can be reduced. This leads to faster, more flexible electronic warfare systems. Stratix series FPGAs with high-speed serial transceivers up to 6.375 Gbps allow enough I/Os to consolidate these functions as a single system on a programmable chip (SOPC), as shown in [Figure 6](#).

Figure 6. SOPC Design Reduces System Latency and Increases Reaction Times

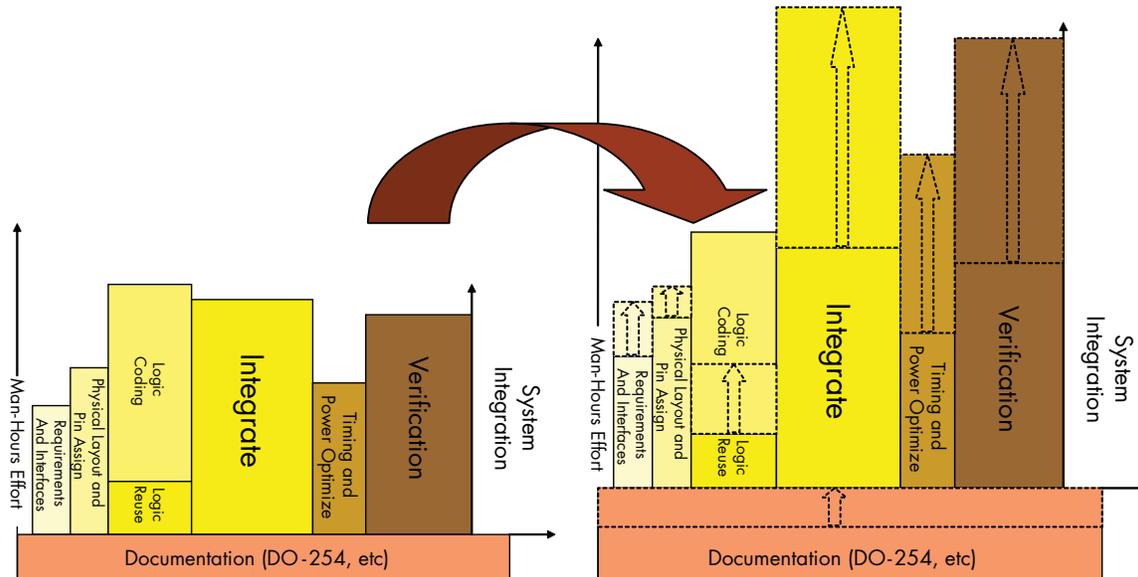


Addressing Design Productivity With High-Density FPGAs

Design architects are looking for ways to take advantage of the faster performance and lower power of FPGA logic in functions traditionally performed only in software. This requires a significant degree of management discipline in managing hardware design, integration, test, and verification. The function of PLDs in military systems has migrated from support and glue logic into advanced signal processing and decision systems. This brings algorithm design and FPGA design closer together, and brings a strong emphasis to design productivity as a cost driver in electronic warfare programs.

Figure 7 shows that as FPGA functions grow and encompass more parts of a military system, they result in growth in the hardware design effort. The largest impacts are in integration, verification, and overall documentation and configuration management.

Figure 7. Design Effort and Schedule Impacts From Increasingly Large FPGA Devices



Thus, it more important than ever to consider the design software flow when selecting programmable logic. Spending needless time on integration, logic block interconnect, compile time, and debugging can cost hundreds of hours of effort. Altera’s Quartus design software, and partner network of synthesis and verification tools (Figure 8), has significant advantages in design productivity.

Figure 8. Compatible Verification and Synthesis Solutions



Getting started on Altera design tools is easy—Quartus II software is the only design solution that includes everything needed for the entire cycle of FPGA and ASIC design for electronic warfare systems. Quartus II software includes DSP Builder block set support for The Mathworks’ MATLAB, SOPC Builder, Power Estimator, Incremental Place and Route, Power Optimizer, and TimeQuest timing analyzer.

Altera’s SOPC Builder is the next tool in the value chain for military designs. Using the proprietary Avalon interface, SOPC Builder easily integrates several partitioned logic systems together, automating interface protocols and bitwidths. SOPC Builder is an excellent tool for encapsulating company IP for reuse from one product design to another.

The Quartus II design suite also includes all of the tools needed to optimize HDL design for implementation on silicon.

Quartus II Design Flow Advantages for Military Electronics Systems

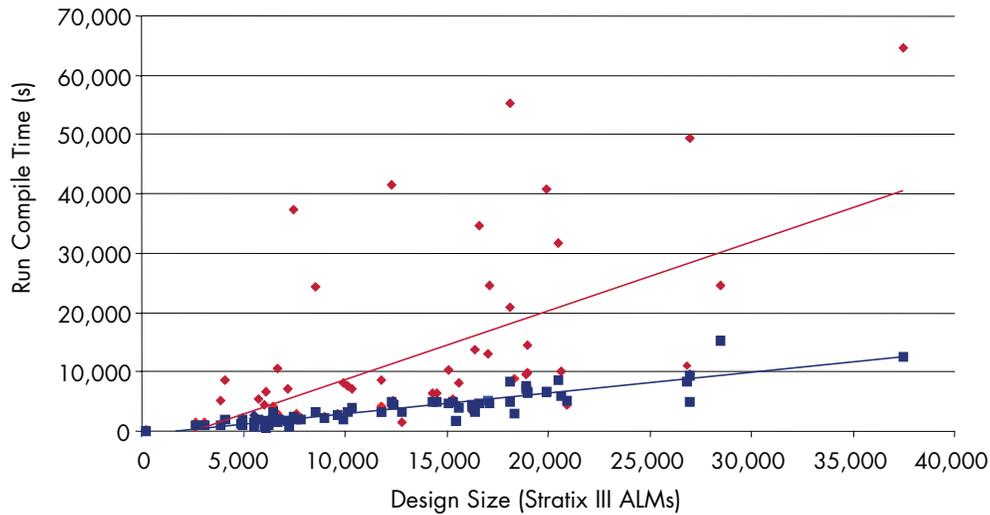
Table 1 shows the numerous features of the Quartus II design suite that improve compile-time performance in military designs.

Table 1. Design Productivity Advantages With Quartus II Design Software

Requirement	Altera Design Solution
Timing support	Only TimeQuest Timing Analyzer offers native support of Synopsys Design Constraint (SDC) standard for timing analysis.
Fast compile times	Common design benchmarks show Altera designs compile twice as fast as the nearest competitor at 65 nm.
	Only Quartus II software supports multi-CPU processors, complete with performance increase benchmarks.
	Quartus II software is only design software with full 64-bit support on Windows OS, supporting more memory (>2 Gbytes) for faster compile times.
	Altera’s simple design partitioning allows for incremental compile and reduction in recompile time by up to 70%.

In addition to the savings-by-design of Quartus II software, options for decreasing compile times include 64-bit Windows OS support, multiple processor support, and Incremental Compile. This feature allows designers to segment large projects at inception into smaller, more easily compiled sections that can be integrated together with a streamlined compile flow. The resulting compilation time savings can be seen in Figure 9.

Figure 9. Compile Times of Stratix III FPGAs vs. Competition Using Identical Designs



Signal Integrity on Digital Interfaces

Signal integrity is an important performance issue for PLDs, as well as all other signal propagation devices in a military sensor system. Very small differences in signal error can have highly magnified effects when propagated through array processing algorithms.

Signal integrity in Altera FPGAs is by design—both in silicon and in FPGA packaging. On-chip termination improves power performance as well as controlling stray voltage, improving signal integrity. Output delay control, on-die capacitors, and slew rate controls likewise improve stray electromagnetic effects that cause signal imbalances. Altera packaging is also designed for enhanced signal reliability with on-package capacitors and optimized pin geometries.

Conclusion

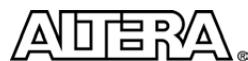
Modular designs of surveillance and electronic warfare systems are now focused on design re-use and interoperability. Aircraft and weapon systems design is no longer the sole function of one design group, but a mindset that must be shared by design architects and digital logic designers. The Altera Stratix series of PLDs and Quartus II design software offer real solutions to the design challenges of electronic warfare systems. From interconnect speed and latency, heat dissipation, design complexity, to lean compile times, Altera products offer advantages that are visible from architectural design all the way to field deployment.

Further Information

- Altera's Military Electronic Warfare:
www.altera.com/end-markets/military-aerospace/ew/ew

Acknowledgements

- J. Ryan Kenny, Technical Marketing Manager, Military and Aerospace Business Unit, Altera Corporation



101 Innovation Drive
San Jose, CA 95134
www.altera.com

Copyright © 2007 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.