Nios II Performance Benchmarks

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Performance Benchmarks Overview

This datasheet lists the performance and logic element (LE) usage for a typical implementation of a Nios® II soft processor and peripherals. Nios II processors are configurable and designed for implementation in Altera® FPGAs. The following Nios II processors cores were used for these benchmarks:(1)

- Nios II/f—The Nios II/f "fast" processor is designed for high performance and has the most configuration options, some of which are unavailable in the Nios II/e processor.
- Nios II/e—The Nios II/e "economy" processor is designed for the smallest possible logic size while still providing adequate performance.

The default options for the Nios II processor were chosen for these benchmarks, unless specified otherwise.

Note: Results may vary slightly depending on the version of the Quartus® Prime software, the version of the Nios II processor, compiler version, target device and the configuration of the processor. Also, any changes to the system logic design might change the performance and LE usage. All results are generated from designs built using the Qsys tool.

The Dhrystone MIPS (DMIPS) reports were obtained using the Dhrystone 2.1 benchmark. You can download the Dhrystone 2.1 benchmark software with the **Fast Nios II Hardware Design Example** on the Altera website. For more information about the Dhrystone 2.1 benchmark software and the Fast design example, refer to the **readme.txt** file which is included in the design example page.

The CoreMark software can be registered and downloaded at *www.eembc.org*.

Note: The Nios II Classic and Nios II Gen2 benchmark data are very similar. The Nios II Gen2 processor was used to create the systems which gave the data values reported in this document. Please refer to the older versions of this document for values associated with the Classic cores.

The resource utilization results were generated using moderate Analysis, Synthesis and Fitter settings in the Quartus Prime software. These results represent typical results.

(1) The Nios II/s core is only available with the Nios II Classic soft processor.

Table 1: System Configuration for Nios II Performance Benchmarks

Benchmark	Nios II Processor	I-Cache	D-Cache	Other options	Peripherals
f_{max}	Nios II/e	None	None	• JTAG debug module (default)	• 64 Kbytes On-chip RAM • Avalon Memory-Mapped pipeline Bridge • JTAG UART • Timer
	Nios II/f	4 Kbytes	2 Kbytes	• JTAG debug module (default) • Hardware multiplier	• 64 Kbytes On-chip RAM • Avalon Memory-Mapped pipeline Bridge • JTAG UART • Timer
Logic size	Nios II/e	None	None	• JTAG debug module (default)	• 64 Kbytes On-chip RAM • Avalon Memory-Mapped pipeline Bridge • JTAG UART • Timer • Avalon UART • SDRAM controller(2)
	Nios II/f	4 Kbytes	2 Kbytes	• JTAG debug module (default) • Hardware multiplier	• 64 Kbytes On-chip RAM • Avalon Memory-Mapped pipeline Bridge • JTAG UART • Timer • Avalon UART • SDRAM controller(2)
DMIPS	Nios II/f at 100 MHz	4 Kbytes	2 Kbytes	• JTAG debug module (default) • Hardware multiplier	• 128 Kbytes On-chip RAM • JTAG UART • Timer
CoreMark(3)	Nios II/f at 100 MHz	32 Kbytes	32 Kbytes	• JTAG debug module (default) • Hardware multiplier	• 128 Kbytes On-chip RAM • JTAG UART • Timer

Related Information

- **Fast Nios II Hardware Design Example**
- **CoreMark Software Download**

(2) The RAM controller for this device is based on DDR3 SDRAM Controller with UniPHY.
(3) This benchmark is compiled with the gcc -o3 switch for optimised performance.

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Table 2: f_{max} for Nios II Processor System (MHz)

Device Family	Device used	Nios II/f[4]	Nios II/e[4]
Stratix IV	EP4S100G5H40I1	240	280
Stratix V	5SGXEA7N2F45C1	340	410
Cyclone V	5CGXFC7D6F31C6	170	220
Arria V GZ	5AGZME7K2F40C3	280	360
Arria V	5AGXFB5K4F40I3	200	250
Arria 10	10AX115U3F45I2LG	270	350
MAX 10	10M50DAF484C6GES	150	160

Table 3: Typical Logic Size for Nios II Processor Cores and Peripherals

Processor Core / Peripheral	Stratix IV (ALUTs)	Stratix V (ALMs)	Cyclone V (ALMs)	Arria V GZ (ALMs)	Arria V (ALMs)	Arria 10 (ALMs)	MAX 10 (LE)
Nios II/f	1151	746	854	750	844	861	2241
Nios II/e	524	289	303	292	314	284	789
Nios II JTAG debug module	165	128	125	123	125	111	368
Avalon UART	95	62	57	56	57	56	143
JTAG UART	114	57	58	58	58	58	159
SDRAM Controller[2]	3825	2666	2466	2616	2473	177	4556
Timer	92	68	56	55	56	58	141

Table 4: Nios II Processor Architecture Performance

Performance Metric	Nios II/f	Nios II/e
DMIPS/MHz Ratio	1.13	0.15
CoreMark	193.3	16.8

[4] Results were generated using push button Analysis, Synthesis and Fitter settings in Quartus Prime.

Related Information

- **AN-440: Accelerating Nios II Networking Applications**
  For more information about the Nios II networking applications performance.
- **Nios II Custom Instruction User Guide**
  For more information about the Nios II floating-point custom instruction performance.
- **Exception Handling**
  For more information about the Nios II interrupt latency performance, refer to the "Exception Handling" chapter of the *Nios II Gen2 Software Developer's Handbook*.
- **AN730: Nios II Processor Booting Methods in MAX 10 FPGA Devices**
  For more information about the Nios II boot process and benchmarking.

Document Revision History

Data	Version	Changes
December 2015	2015.12.16	• Updated to 15.1 release • Arria10 and CoreMark results added